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SIGNAL PROCESSING STUDIES PROGRAM VLSI DESIGNS FOR UNARY FUNCTIONS BY: JH HARRIS

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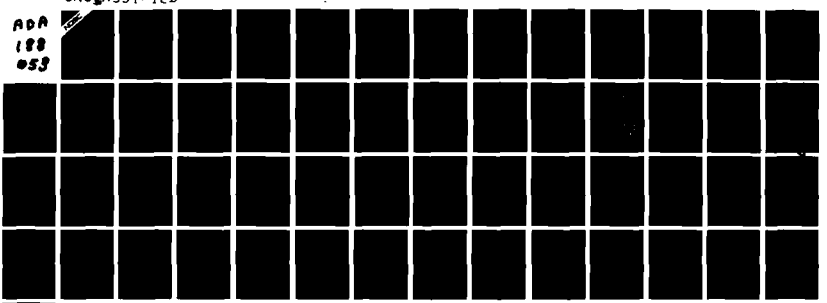

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Technical Document 1162
September 1987

Signal Processing Studies Program VLSI Designs for Unary Functions

J. H. Harris
San Diego State University Foundation

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This report was prepared by San Diego State University Foundation under contract N66001-85-D-0203 for Code 74 of the Naval Ocean Systems Center.

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Signal Processing Branch

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and Technology Division

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SECURITY CLASSIFICATION OF THIS PAGE

REPORT DOCUMENTATION PAGE

1a REPORT SECURITY CLASSIFICATION UNCLASSIFIED	1b RESTRICTIVE MARKINGS
2a SECURITY CLASSIFICATION AUTHORITY	3 DISTRIBUTION/AVAILABILITY OF REPORT Approved for public release; distribution is unlimited.
2b DECLASSIFICATION/DOWNGRADING SCHEDULE	
4 PERFORMING ORGANIZATION REPORT NUMBER(S)	5 MONITORING ORGANIZATION REPORT NUMBER(S) NOSC TD 1162
6a NAME OF PERFORMING ORGANIZATION San Diego State University Foundation 6b OFFICE SYMBOL (if applicable) SDSU	7a NAME OF MONITORING ORGANIZATION Naval Ocean Systems Center
6c ADDRESS (City, State and ZIP Code) 5178 College Avenue San Diego, CA 92182	7b ADDRESS (City, State and ZIP Code) San Diego, CA 92152-5000
8a NAME OF FUNDING/SPONSORING ORGANIZATION Office of Naval Research 8b OFFICE SYMBOL (if applicable) ONR	9 PROCUREMENT INSTRUMENT IDENTIFICATION NUMBER N66001-85-D-0203
8c ADDRESS (City, State and ZIP Code) 800 N. Quincy Arlington, VA 22217-5000	10 SOURCE OF FUNDING NUMBERS PROGRAM ELEMENT NO: 61153N; PROJECT NO: EE55; TASK NO:; AGENCY ACCESSION NO: DN088 669

11 TITLE (Include Security Classification)
Signal Processing Studies Program VLSI Designs for Unary Functions

12 PERSONAL AUTHOR(S)
J.H. Harris

13a TYPE OF REPORT	13b TIME COVERED	14 DATE OF REPORT (Year, Month, Day)	15 PAGE COUNT
Interim	FROM Jan 1987 TO Jan 1987	September 1987	57

16 SUPPLEMENTARY NOTATION

17 COSATI CODES			18 SUBJECT TERMS (Continue on reverse if necessary and identify by block number)
FIELD	GROUP	SUB-GROUP	interconnecting cells Mosis cells bounding box polysilicon rectangles

19 ABSTRACT (Continue on reverse if necessary and identify by block number)

This report deals with the need for special purpose chips for future high performance signal processing applications, an examination into the nature of the enhancement in efficiency provided by a competitive workstation.

20 DISTRIBUTION/AVAILABILITY OF ABSTRACT	21 ABSTRACT SECURITY CLASSIFICATION
☐ UNCLASSIFIED/UNLIMITED ☒ SAME AS RPT ☐ OTIC USERS	UNCLASSIFIED
22a NAME OF RESPONSIBLE INDIVIDUAL J.J. Symanski	22b TELEPHONE (Include Area Code) 619-225-2200
22c OFFICE SYMBOL Code 74	

DD FORM 1473, 84 JAN

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A VLSI STANDARD CELL LAYOUT

J.H.Harris

Use of engineering workstations greatly facilitates the design of special purpose (application specific) electronic circuits of VLSI level complexity. With a view toward the likely need for special purpose chips for future high performance signal processing applications, an examination into the nature of the enhancement in efficiency provided by a competitive workstation was conducted using the Chipmaster software available on a Daisy workstation. Layout of an "on-line" arithmetic circuit was performed. The circuit implements an algorithm for computing 1/X where X is the binary input to the circuit. "On-line" refers to arithmetic methods in which the results of computations are obtained in the form of a sequence of digits with the most significant digit obtained first and succeeding digits obtained in turn. "On-line" algorithms have been developed by Ercegovac[1], the logic level circuit used in the study was generated by Henderson[2], and the effort was part of a broader study of systolic array signal processing systems by Symanski[3].

Layout consisted of placement and routing of standard cells organized in essentially a channel configuration. The cell library

was obtained from the Mosis program at USC. The layout effort was viewed as a trial program intended to uncover elements of design methodology and there was no intention to implement the circuit by fabricating the chip. The utility of the algorithm itself for systolic array applications has not been addressed. Had the intent been to fabricate the chip, the Mosis program could have secured mask making and foundry facilities and produced samples using the data generated on the workstation. Spice simulations performed as part of the study have indicated that the inherent delays of the cells are in the nanosecond range, which is sufficient for current applications.

THE MOSIS CELLS

The Mosis standard cells used in the study consist of 3 micron gate length CMOS devices of moderate logic gate level complexity. The gates range from AND and OR gates with a few inputs through Exclusive-OR gates and D flip-flops. The structure of the devices is illustrated in Figure 1 where the full layout for a two input AND gate and a three input NOR gate are shown in stipple pattern. The metal and polysilicon layers are highlighted in the figure. The layouts contain no buried (diffusion to polysilicon) contacts. All contacts are to metal.

A principal feature of the cells is their large gate widths which

results in a large overall standardized cell height (120 microns). The p-chanel pull-up transistor widths are somewhat larger than the pull-down widths, partially compensating for the timing differential that results from a two-to-one ratio in peak saturation current that itself is due to the difference between p- and n-channel mobility. Inputs and outputs of the cells are polysilicon, facilitating a structured grid layout in which interconnections are made by first creating a metal line that passes between gates and then extending polysilicon connections to the metal line. It was found very convenient to prepare the cells by having an indicator of inputs and outputs. These may be seen as the small markings on the ends of the polysilicon regions in Figure 1. Note that the inputs to the NOR and NAND gate are equivalent and have the same indicator.

The pricipal impact of having large transistor widths is an increase in the size of the cells and a reduction in the number of gates that can be put on a chip. At the same time, however, the large cells reduce the impact of interconnect loading on timing delays and work to assure the avoidance of unexpected delays. The basis for this improvement in performance reliability is that gate delays in integrated circuits can be largely attributed to the time required to change the voltages on capacitive loads that appear on the outputs of the gates. The loads consist primarily of the capacitance of the inputs to other gates to which the prescribed gate "fans-out" and the capacitance of the metal interconnect. The time to change the voltage on a capacitor may be expressed

$$T=CV/\langle I\rangle \qquad (1)$$

where C is the load capacitance, V is the volatge swing between logic values and $\langle I\rangle$ is the average drive current (actually the average of 1/I) when the device is switching. A typical value for $\langle I\rangle$ is 1/2 to 2/3 the maximum saturation current Isat. Isat may be expressed in terms of physical parameters as follows

$$Isat=(uCox/2)[Vdd-Vt]\ (W/L) \qquad (2)$$

where u is the channel mobility, Cox is the gate oxide capacitance, Vdd is the supply voltage, Vt is the magnitude of the device threshhold voltage, and W/L, the factor of primary concern, is the width to length ratio of the gate of the driving transistor.

The fan-out portion of the capacitive load is the product of the oxide capacitance Cox and the total area of the fan-out gates. The fan-out capacitance may thus be expressed

$$Cf= NWLCox \qquad (3)$$

where L, the gate length, is assumed to be the same for all devices and N is the ratio of the total fan-out width to the width of the drive transistor. The other part of the capacitive load is the interconnect capacitance. The interconnect capacitance is the product of the area of an interconnect line and, typically for

current technology, the oxide capacitance per unit area divided by 30. The interconnect capacitance may thus be expressed

$$Ci = (1/30)L'W'Cox \qquad (4)$$

where L'W' is the area of the interconnect. Interconnect lines have a width that is typically at least twice the length of the transistor gates and a length that can be hundreds of microns. The area can thus be large enough to provide a substantial capacitive load despite the factor of 30. When the capacitive loads are combined and indicated values for $\langle I \rangle$ and W' are employed, the resulting gate delay becomes

$$T = [3V/(Vdd-Vt)\,](L/u)(N+L'/15W) \qquad (5)$$

The argument that cells containing transistors of large gate width W have reduced impact due to interconnect capacitance is well demonstrated by the appearance of the term L'/W in equation (5). In addition, the equation illustrates the preeminent role of the mobility and gate length in determining the timing properties of VLSI circuits. The magnitude of the delay expressed in (5), taking the p-channel mobility (200 cm /v-sec) and 3 micron gate length L into account, is of order

$$T=(0.4)(N+L'/15W) \text{ nanosec.} \qquad (6)$$

Although various other factors contribute to the delay, the heart

of the matter is expressed in (6). A good design with limited fan-out and interconnection lengths that are not too large a multiple of the output transistor gate width can have individual gate delays of the order of nanoseconds. Many Mosis cells have a width comparable to W. As a rule of thumb, we may note that the interconnect capacitance becomes a significant problem when the output bus exceeds a length of 15 cells.

Methodology Issues

The layout of a circuit consists of arranging and interconnecting cells and is referred to as the placement and route problem. The object is to obtain short interconnecting paths and as close an overall packing as possible. Software ia available for performing this function in automatic fashion, based in large part on cut-and-try methods, but the layout of the "on-line" chip was performed by hand. The layout configuration is structured on the low end by the orientation of the cells and on the high end by the hierarchical nature of the circuit.

The cells are oriented so that when they are aligned side by side the supply voltage and ground are automatically connected to each cell. This feature makes it convenient to arrange the structure in the form of blocks containing cells that lie side by side. It also makes it convenient to route interconnections between cells in a

block with metal wires that run parallel to the cell width. Fig. 2 is a block of this kind. The metal lines are connected to the cells by relatively short polysilicon lines that serve to extend the gate inputs and outputs.

When routing a block, the objective is to occupy as few routing lanes as possible, in order to keep the overall size small. The arrangement of the cells within the block has a signifacant effect on the number of lanes. If the block contains several parallel circuits and if it is desired to maintain a single line of cells, then cells in each parallel grouping should be placed adjacent to each other in order to minimize the number of interconnects that pass completely over a cell grouping. In this way many interconnections are kept short and each lane can be used for a nuber of interconnections, which is the way in which the overall size of the structure can be kept small.

The schematic itself generally provides a useful intuitive approach to the cell layout done by hand on a workstation. One procedure that can save considerable time is to take a sheet of a schematic and assign a number in sequence to each gate. As discussed above, gates that lie in some sense in series and are interconnected should be numbered sequentially. This number will represent the cell placement in the layout, assuming that all the cells of a page of a schematic are eventually to be placed adjacent to each other. If there is a clear set of parallel groupings in the schematic, then it is advantageous to arrange the cells in two or more

parallel groups. In this case two numbers or an indexed number might be assigned to each gate in the schematic. Thus a gate might be labelled C5 meaning that the cell that implemements that gate will end up as the fifth gate in row C of the schmatic.

After numbering each gate on the schematic, each net should be assigned a number. A net refers to a gate output and all the gate inputs to which it is connected. The number assigned to each net will represent the lane in the channel that will be occupied by the interconnect. Since there are at least two channels (above and below the cells) in each block, the number assigned to each net should also be indexed in accordance with the channel in which it will be placed. The process of assigning a net number is an important part of the process of developing an efficient design. The same net number can be assigned to more than one net, but only one net can occupy the region between the highest and lowest gate number associated with a net number. The number of lanes required depends on the way in which the gate and net numbers are assigned. For example, the two internal interconnections of the simple gate structure shown in Fig.3 occupy only one lane if the OR gate is assigned a number between that of the two AND gates. On the other hand, the interconnections to other elements is likely to determine whether or not any real saving in the number of lanes is achieved by such an assignment. Often clock and enabling lines run the length of a block and these nets may be assigned early in the process. When numbering the nets it may also prove useful to add an index to gate inputs to indicate which of the equivalent inputs

of a gate will be assigned to a specific net.

The process of using the workstation to create a block involves selecting a cell from the library and placing it at a prescribed position on the screen. When the gates are numbered, the process of describing the cell and placing it in the right position can move rapidly. A very useful procedure to follow before generating the layout is to make a list on the schematic of each gate by the number that appears on the schematic and then assign the library number of the cell to the gate number. The resulting gate and library list is useful in checking the layout for error after the layout is completed. Sometimes it is apparent from the schematic that it is useful to reorient a cell so that the output appears on the left side rather than the right or vice versa. This is accomplished with a simple command from the workstation menu. When the cells are all placed it is useful to add script to the screen toindicate the cell number. This facilitates the interconnection process and makes it easier to check the result.

The interconnections are made by running metal wires with appropriate width and spacing parallel to the top of the cells. The number of metal lines is equal to the number of different net numbers. Polysilicon rectangles are then run from gate inputs up (or down) to the metal line indicated by net number on the schematic. Next, predesigned metal to polysilicon interconnects are placed at the intersection of polysilicon and metal lines. The final step is to cut the metal lines wherever more than one net

occupies the same lane and to cut off the ends of the metal lines anywhere they extend beyond the gate input or output to which they are connected. A well trimmed block is probably the most useful element to have available for the next higher level in the hierarchical design where interconnections between blocks are made.

Blocks created from logic gate level circuits are stored in the workstation as a cell and can be incorporated in circuits of greater complexity as a unit. Perhaps the principal feature of the chipmaster software is that it facilitates hierarchical design. The description of a full circuit is of course a listing of the size, position, and mask assignment of basic rectangles that eventually define regions of different material in the transistors in a circuit. A cell represents a grouping of the rectangles. Cells are nested to produce a hierarchical design. The Chipmaster software enables previously created cells to be included in another cell as either a unit that cannot be further manipulated, i.e., no transistors can be removed, or as a transfer cell that can be further altered. In either case the basic rectangles themselves, or the cells as represented by a rectangle of appropriate size, may be viewed on the screen. As the complexity of the circuit grows it takes an increasingly longer time to produce the picture of the circuit at the basic rectangle level on the screen. Each change in the circuit requires redrawing on the screen and it is therefore efficient to work with a circuit in which as many cells as possible are described by a representative rectangle, referred to as a "bounding box" by Daisy. If the input and output options of the

bounding box are planned in advance of generating the layout at higher levels, the process of generating the layout at the higher levels can be simplified.

As the nesting or hierarchical level of the design increases, there is generally an increasing geometric variation in the size and shape of the cells that are placed in the design. Enhanced deviation is expected as the number of elements grows. The variation in size and shape increases the complexity of both the placement and route problems. Dealing with this complexity when generating a layout on a workstation is aided if there is a global view of the circuit so that when the blocks are developed they can be designed to take advantage of special situations. For example, one situation that may arise is the appearance of a substantial number of connections between identical blocks. The outputs of certain cells in a block will thus provide the inputs to other cells in a replicated version of the block. The situation is illustrated in Fig.4. When the block is being designed the lower level cells can be placed so that associated inputs and outputs are located near each other. If the input and output interconnections of blocks that are replicated many times are assigned net numbers and the associated gates are assigned close numbers, the goal of minimizing the area taken up by interconnections between identical blocks can be facilitated.

Of necessity, the designer of the logic level circuit has a picture in mind of the hierarchical organization of the circuit. He is in

a good position to structure the higher level layout and it is wise to have him at least participate in the layout process. One way to do this that should prove simple and effective is to have him prepare a plan of the circuit in the form of a block diagram that is sketched to approximate size. This can be done adequately by assuming a uniform dimension for each gate. Interconnections between blocks would be shown. Such a top level view of the circuit can be of substatial help in layout design which is necessarily a bottom-up process.

THE CHIP LAYOUT

Work completed on the project appears in Figs. 5 and 6. Fig. 5 contains cells in which some degree of nesting is demonstrated so that cells created for the project are represented in the layouts by bounding boxes. Fig. 6 shows the same cells but includes the full layout to the polygon level. Only cell JA11 appears exclusively at the polygon level. A pair of inverters (contained in a single standard cell) and two NOR gates make up cell JA11. The cell designation (e.g, JA11) refers to the cell series JA and page 11 of the original logic gate level description of the circuit.

Fig. 5A, cell JA1, shows the highest level description of the circuit. As mentioned previously, the circuit was not completed, but more than half the elements are contained in JA1. JA1 is seen

to contain two regions each of which is approximately 2,000 by 3,000 microns or 6 square millimeters in area. One of the regions is a defined cell contained within the bounding box labelled JA6 and the other is the multiple replication of cell JA7. Overlap of the bounding boxes representing JA7 does not imply overlap of the cells themselves as is evident in Fig. 6. The relative placement of the regions is not optimized as it depends on the portion of the circuit not completed. The transistor level layout of the replicated JA7 cells is shown in Fig. 5B.

The two cells JA6 and JA7 that appear in JA1 are shown next. JA6 itself consists primarily of a number of replications of the cells JA9 through JA12 including a modification of JA10 designated as JA102. Those cells designated with an X, such as appear in Fig.5c are the standard cells of the Mosis library. Three versions of cell JA7 are shown to illustrate different hierarchical representations for the cell. In one JA8 appears. JA9 is a cell contained within JA8 which is evident in the second representation of JA7. The third representation shows detail of the interconnection of several component standard cells.

Cells JA8 through JA12 are of differing degrees of complexity with the simplest cell being JA11. The layout for JA11 shows the use of lettering to indicate block level inputs, metal interconnections in channels above and below the standard cells, and special symbols to specify inputs and outputs of the individual standard cells. In several of the cells, input and output lines are brought out to the

cell boundaries. As discussed in the previous section, it is probably preferable to have connections to a block made at a higher level and to not bring connection points out to the cell boundary since this tends to restrict placement and orientation of the cell at the higher level.

SPICE SIMULATION

A spice data file was established for the purpose of simulating the electrical behavior of representative Mosis standard cells and verifying their timing characteristics. CMOS transistor model data provided by Mosis was used and is shown in Fig.7. Interest was focused on the D flip-flop with clock and reset control, which was the most complex of the cells. The transistor level circuit of the flip-flop is shown in Fig.8. The Spice data file for the flip-flop, which is presented in Fig. 7, was structured so that the inverter and inverter-like circuits that comprise the device could be removed readily from the description to enable part of the circuit to be examined or to deal with computational difficulties. The flip-flop and associated clock drive circuit contain 31 transistors.

Examples of the results of simulations are shown in Figures 9 through 12. Figures 9-11 illustrate aspects of the speed of response of the flip-flop subcircuits and show the nature of the

deterioration in response at very high input data rates. Fig.9 shows the response of some cells elements when the input rise, fall, and dwell times are all 1 nanosecond, corresponding to a 250 MHz data rate. The circuit is responds with adequate fidelity and exhibits a delay of 1.4-1.5 nsec. When the time increments are reduced to 60% their value (0.6 nsec.), corresponding to 400 MHz, the circuit no longer responds adequately. Voltage levels do not pass through logic threshhold values. Fig. 10 shows the voltage transfer for the same circuit but with the widths of the cells reduced from that of the oversize Mosis cells to a uniform 6 microns. The behavior of the circuit is similar to that of the circuits with wider (30-50 micron) gates, although the deterioration is marginally more severe at 400MHz. The same circuit was used to generate Fig. 11 which shows the behavior of the pull-up and pull-down currents at internal nodes of the three inverter shift register portion of the flip-flop. Rapid fluctuation in the current at the pulse edges may be observed. These fluctuations, which are due to (Miller) capacitive coupling through the gates, introduce computational difficulties that hamper the ability to simulate more complex circuits.

Figure 12 shows an example of the simulation of the full 31 transistor flip-flop. The clocking in of a low and then a high logic level is shown. Both values arrive after the leading edge of the clock pulse but before the trailing edge. The output of both the master section of the flip-flop and the slave section behave properly, although the output high is somewhat less than the supply

voltage. The output starts to change value when the clock approaches zero volts and the delay, when measured at the logic threshhold level, is approximately 4 nsec.

The simulation shown in Fig.12 is an example of the situation in which two zero impedance sources are varying simultaneously in a circuit that has a substantial number of elements and feedback loops. Simulations of that kind can require substantial computer time. Determination of such flip-flop characteristics as set-up and hold times requires iteration of computations like the one shown in Fig.12. Future simulation needs will require establishing methods such as adding small resistors to the circuit to limit current fluctuations in order to limit the CPU time needed for performing the simulation.

CONCLUSION

The use of a standard cell library like the Mosis library and Chipmaster level engineering workstation facilities provide adequate capability to generate layout designs of VLSI circuits of substantial complexity in modest time. A key to the capability lies in fully documenting the process of preparing the logic gate level description for layout prior to engaging the workstation. With the availability of the workstation, inclusion of fabrication of special purpose chips into signal processing system activities is

feasible. The additional step of verifying that the Mosis program can deliver working chips in reasonable time must be checked to be certain that this can be done rapidly and reliably. Future systems are likely to contain application specific circuits.

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2. T.A. Henderson, On-line square root circuit, NOSC internal report. SAN DIEGO, 1986

3. J.J. Symanski, Implementations of matrix operations on the two-dimensional systolic array testbed, Proc. SPIE. San Diego, Aug. 1983

FIGURE TITLES

1. Sample Mosis cell layouts. a) Two-input AND gate with isolated metal layer to the left. b) Three input NOR gate with metal layer to the left and metal plus polysilicon layers to the right.

2. Sample circuit block composed of standard cells.

3. Gate level circuit with gate numbers assigned. Lower assignment may require a wider channel.

4. Placement of cells in a block that is connected to replicas of the same block (as in cell JA11 Fig. 6). The upper placement is preferred.

5. Plots of subcircuits for on-line square root circuit. Cells demonstrate nesting (hierarchical) properties.

6. Layouts of subcircuits completed for on-line square root circuit.

7. Spice data file describing transistor model characteristics and D flip-flop subcircuits.

8. Circuit for D flip-flop showing node and subcirccuit numbers.

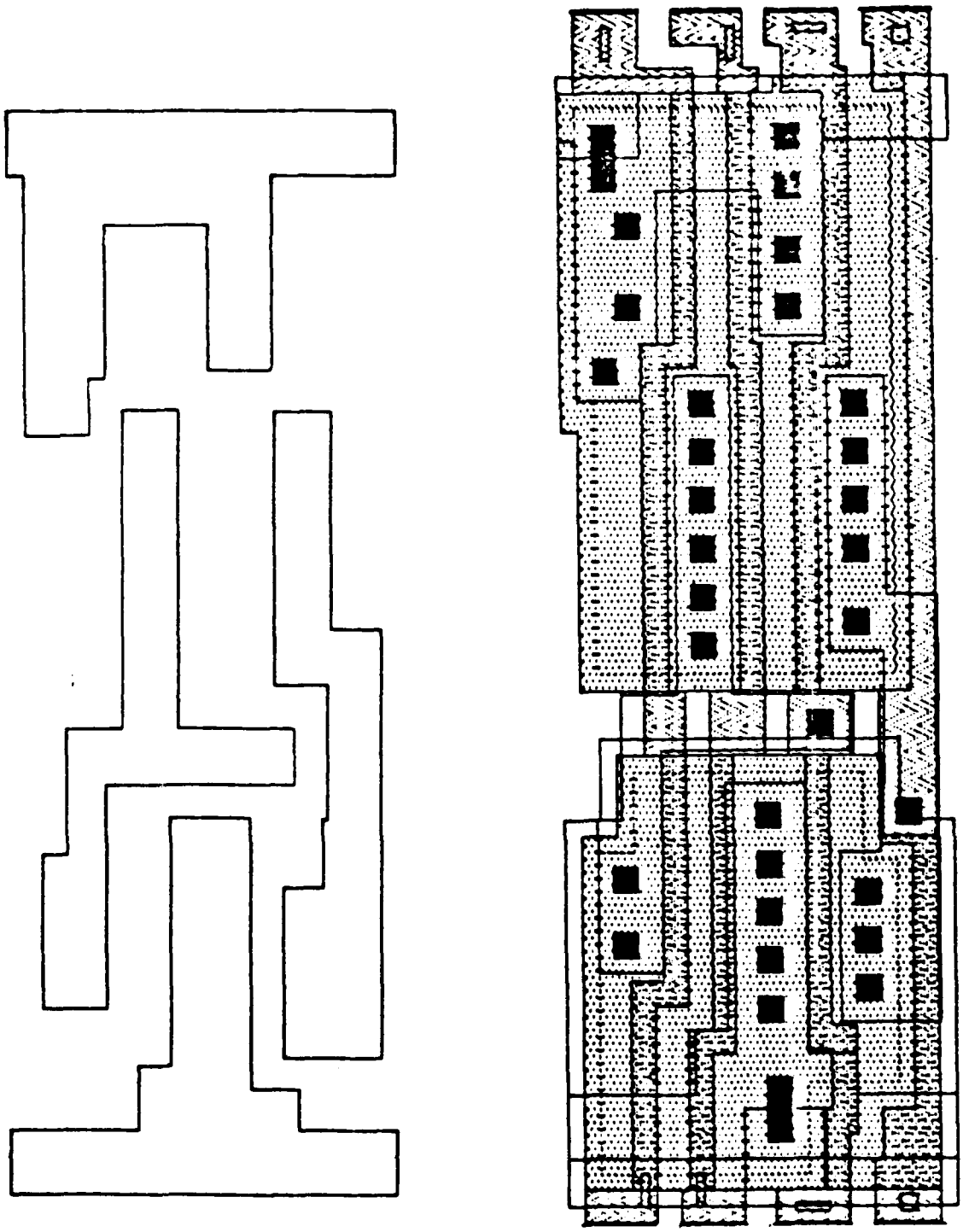
9. Computed time response of first three subcircuits of D flip-flop (see insert). Voltage at the input and at two internal nodes is

shown. The time scale is at the bottom.

10. Time response of circuit of Fig. 9, but with all transistor gate widths reduced to 6 microns.

11. Time response of circuit of Fig. 9 with current fluctuations shown.

12. Clocking of data through the D flip-flop. The signal (blue) arrives after the clock (red).



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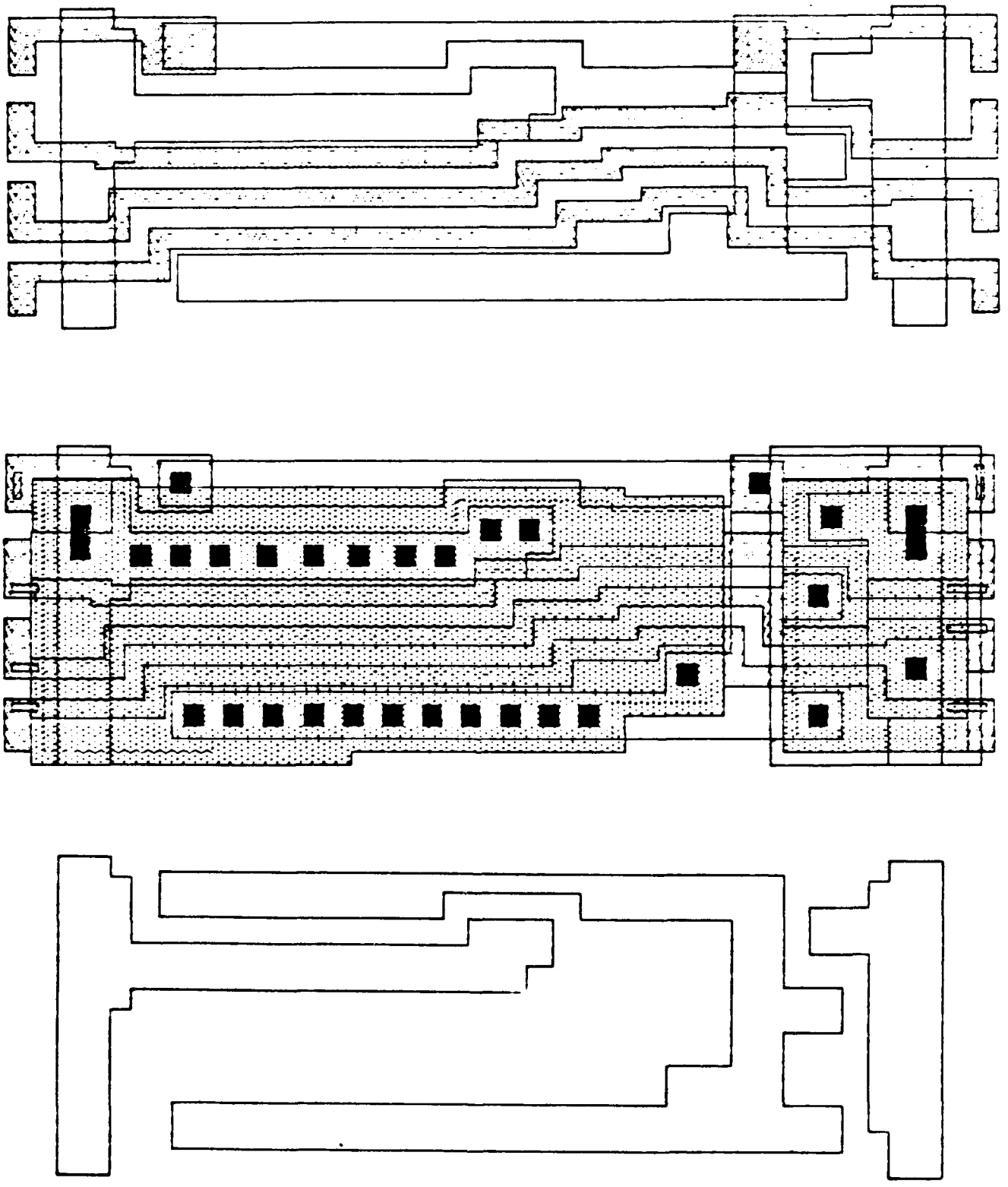

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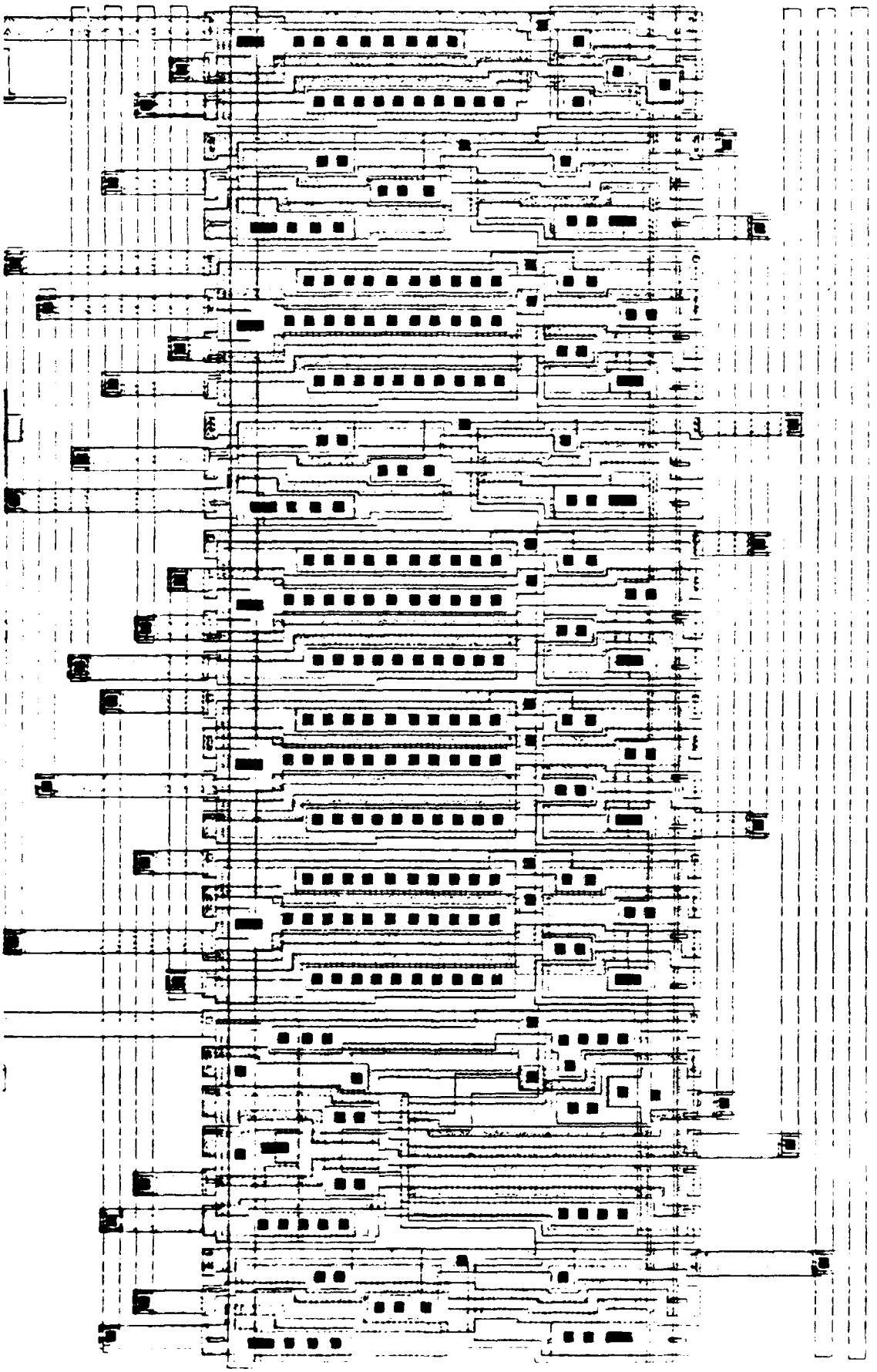

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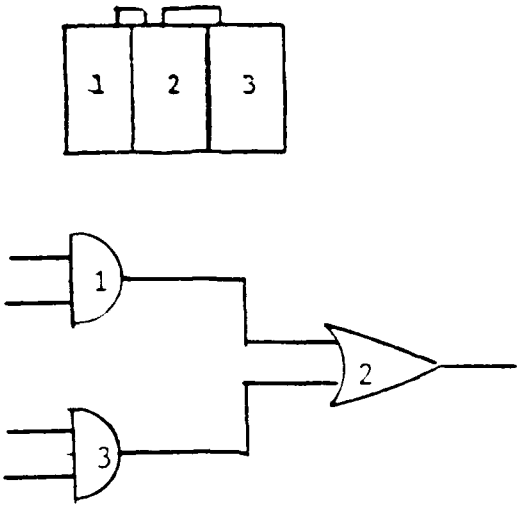

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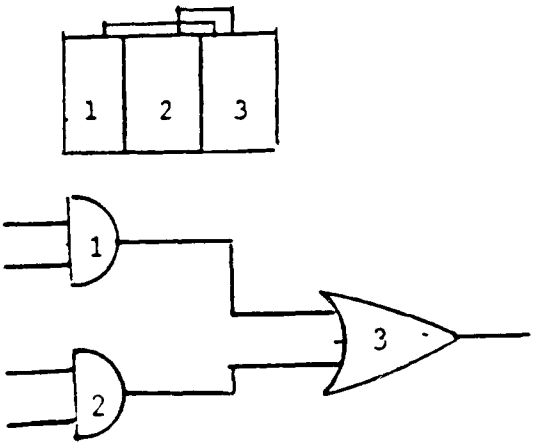

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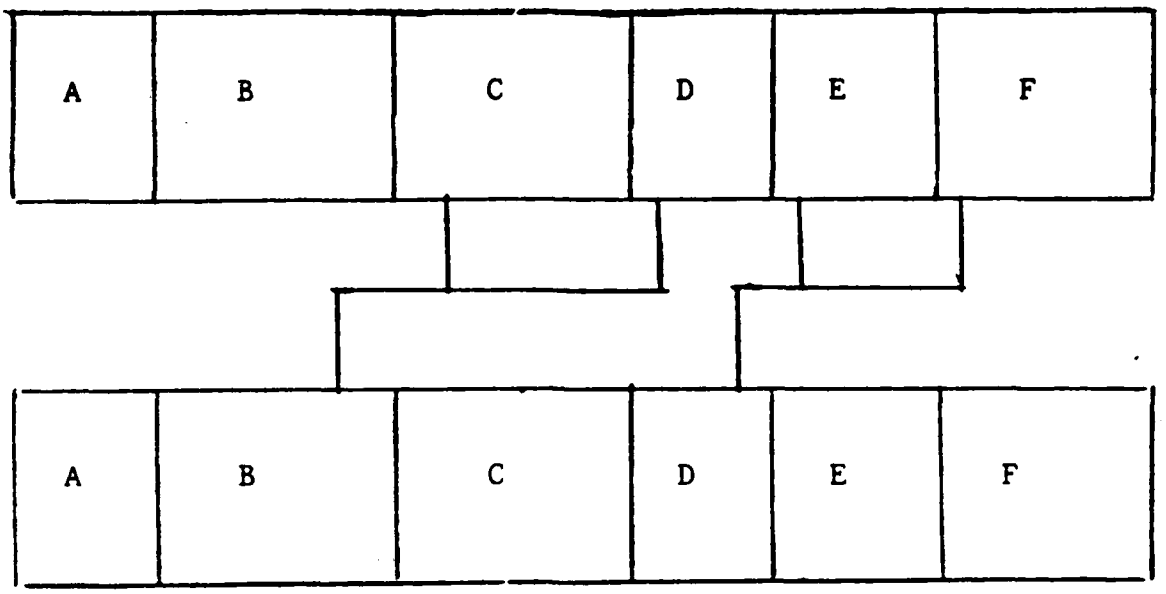

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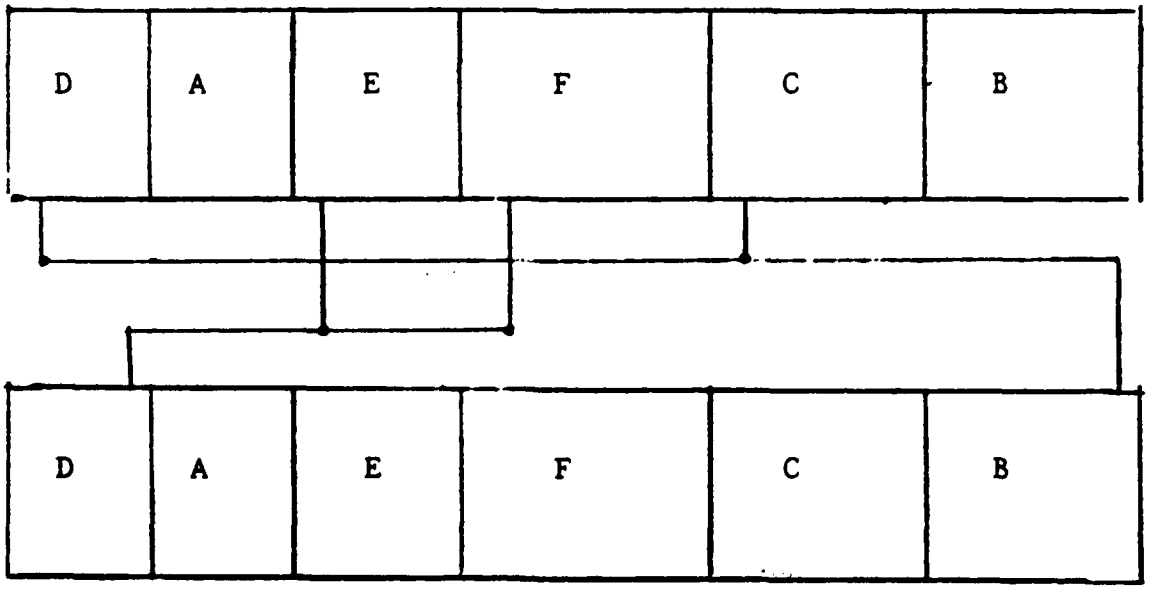

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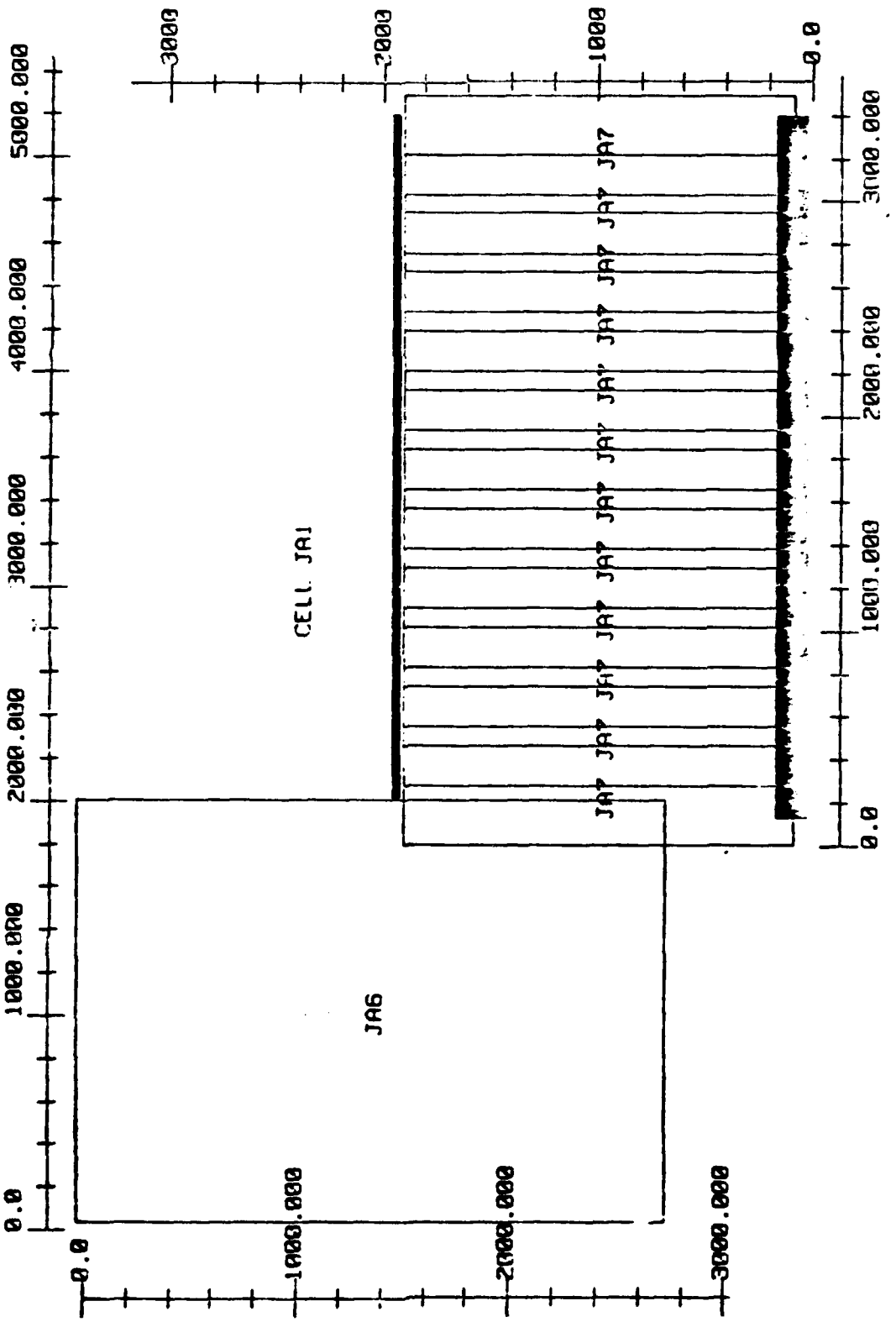
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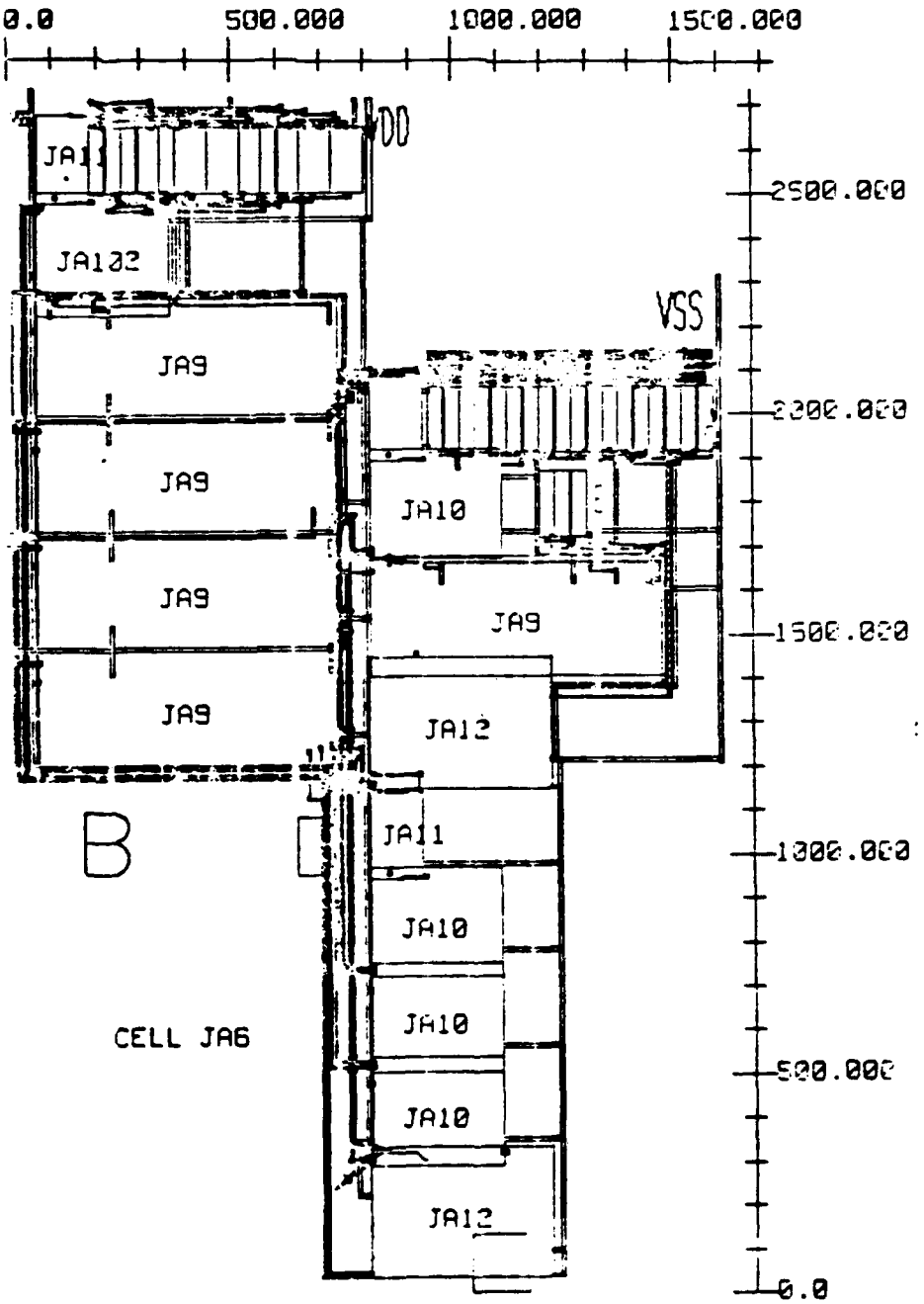
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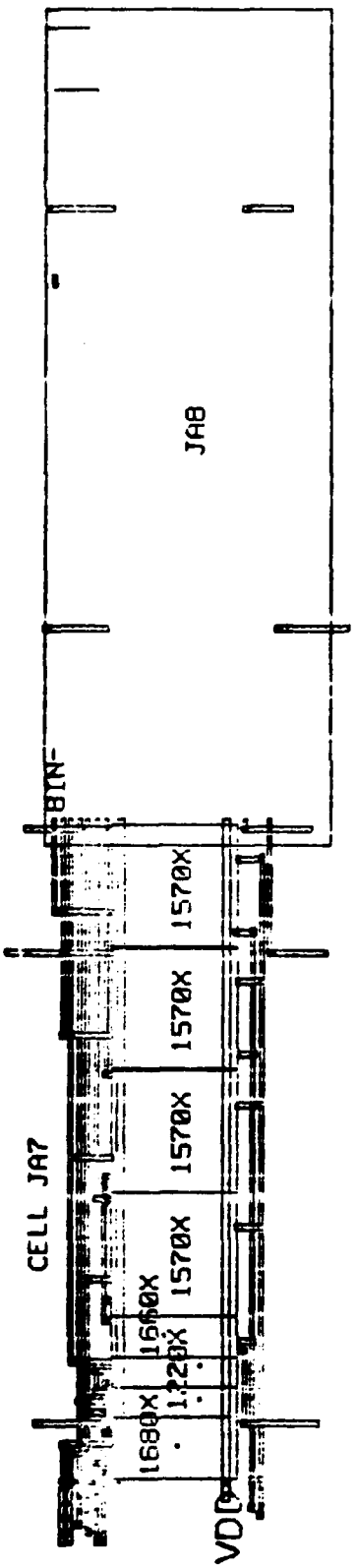
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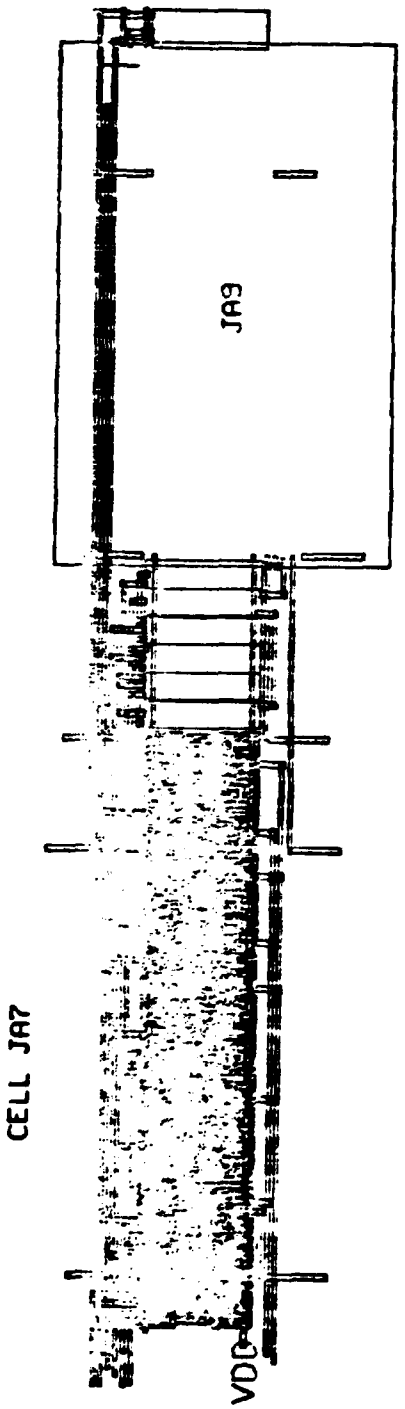
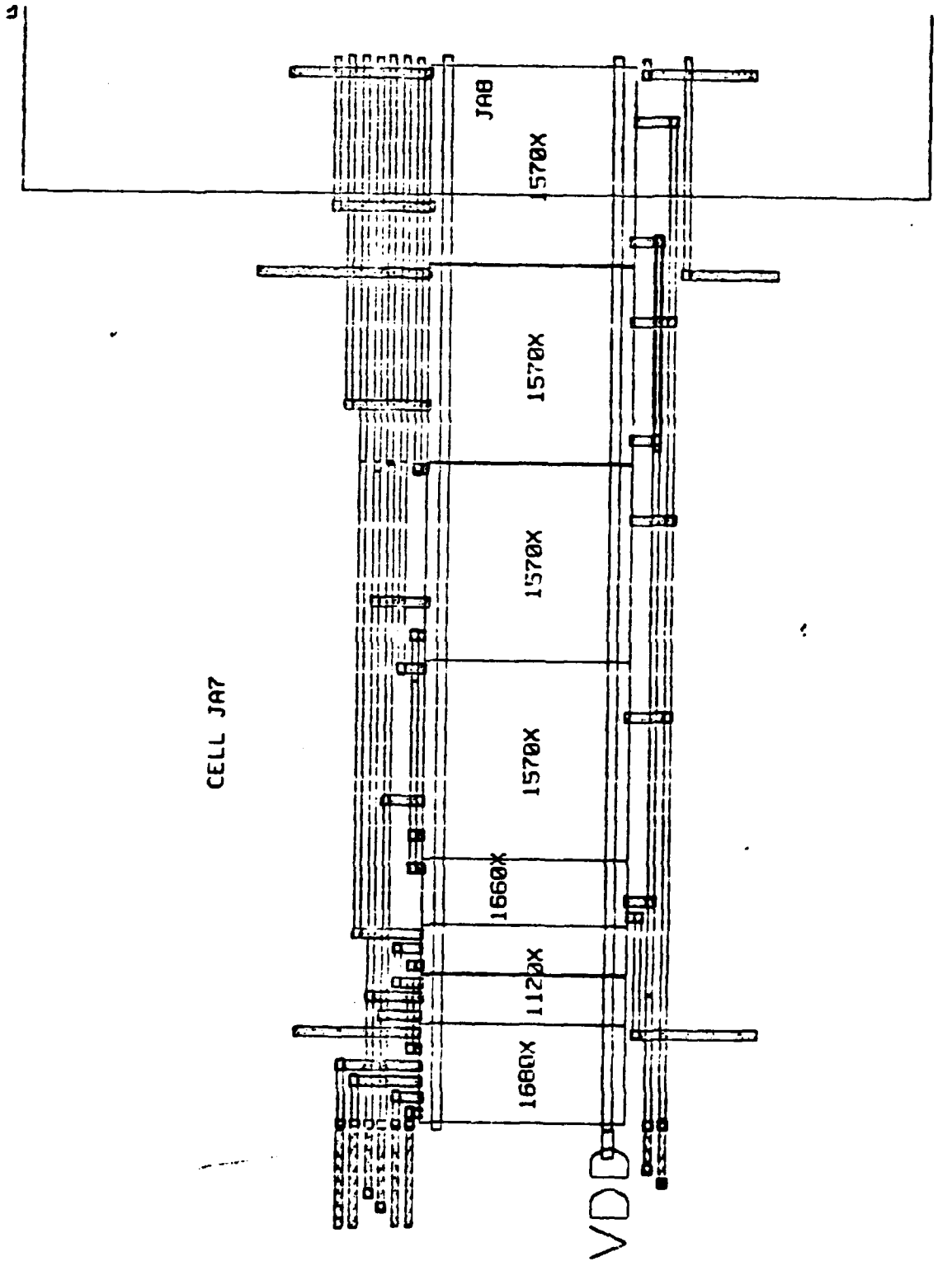
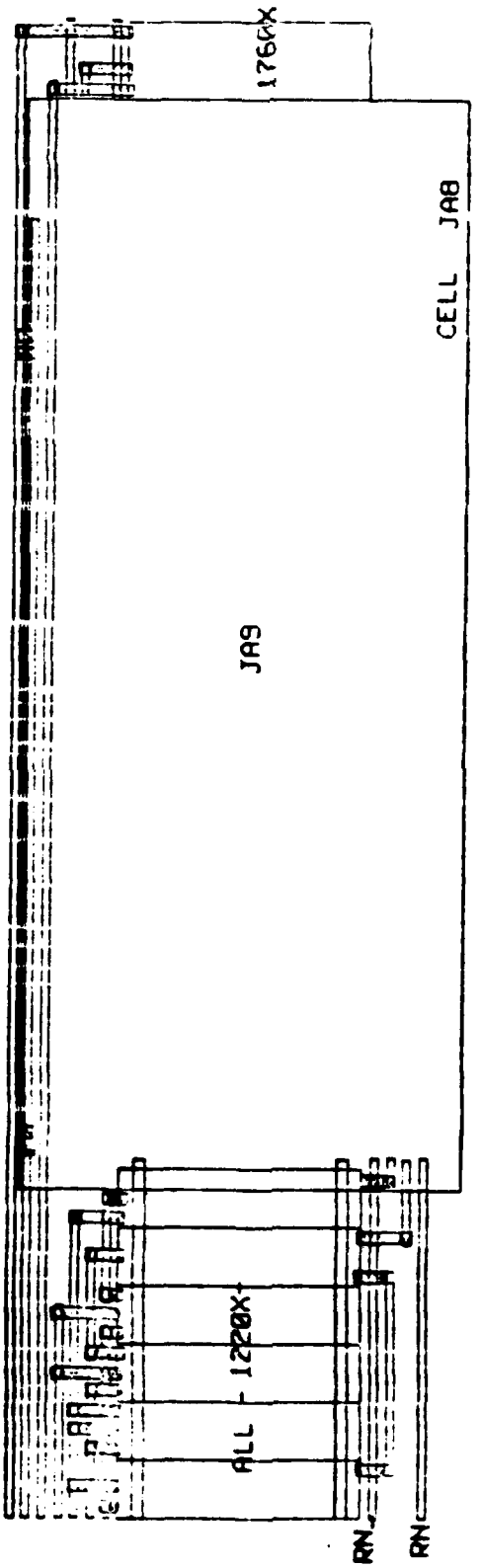
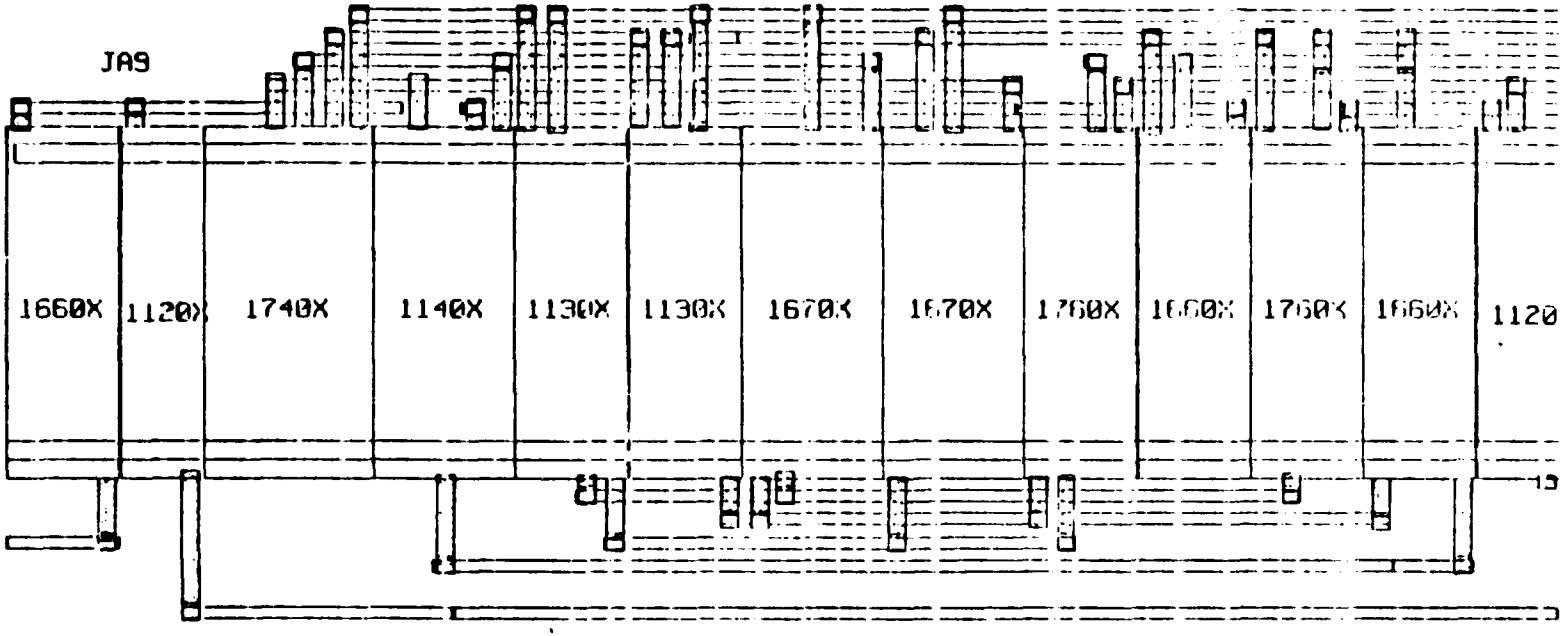
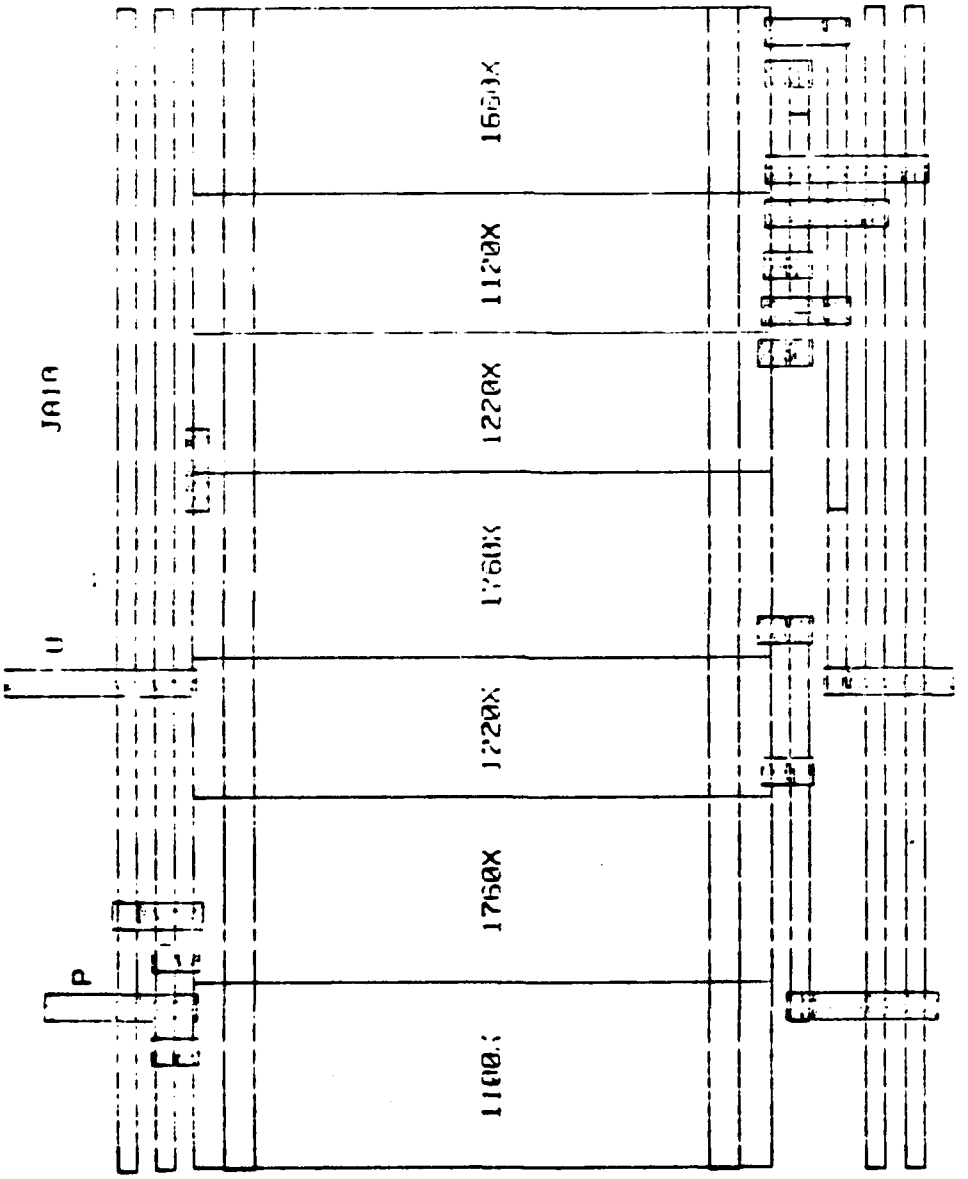
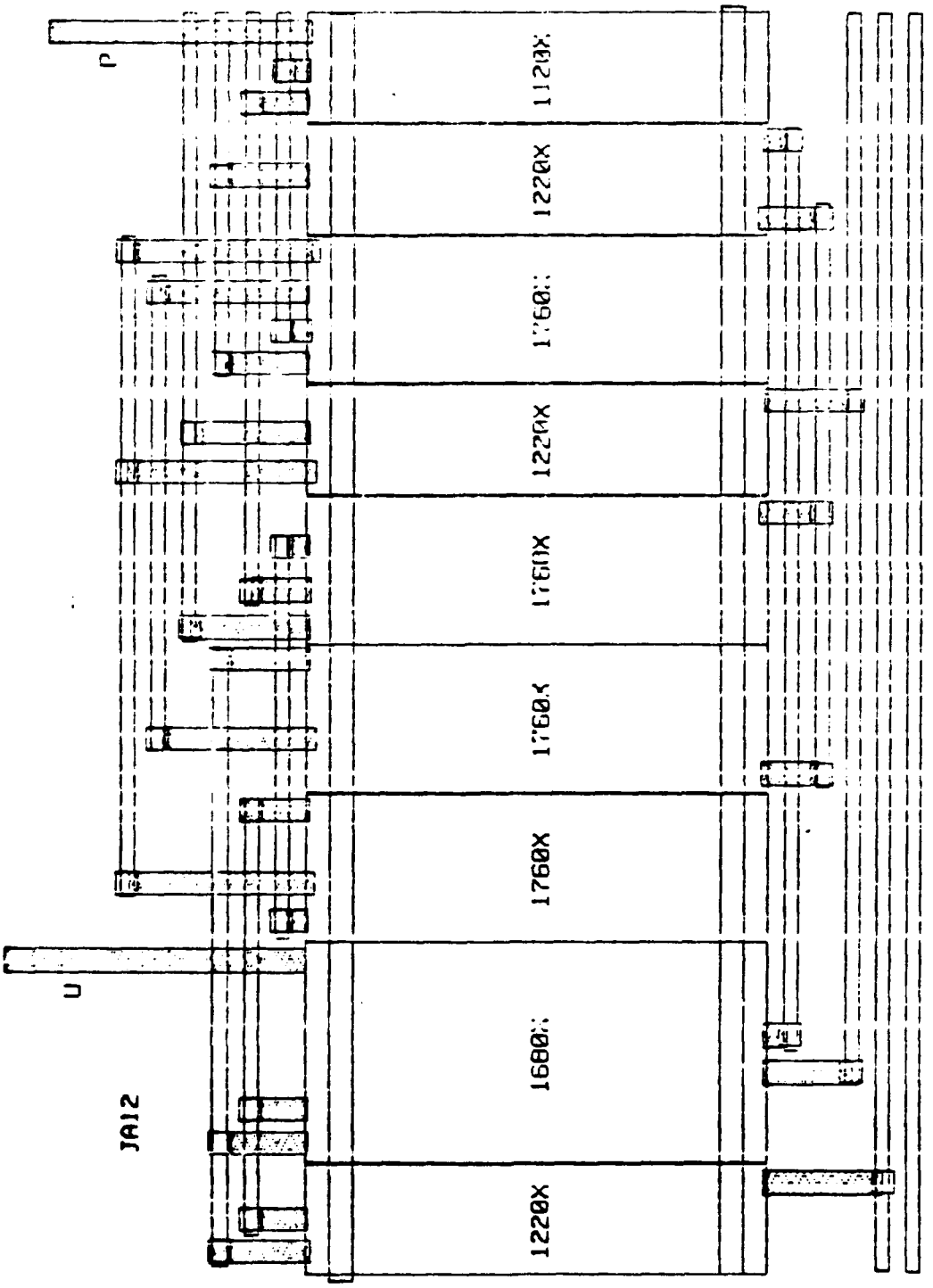

JA9
CELL JA7
VDD

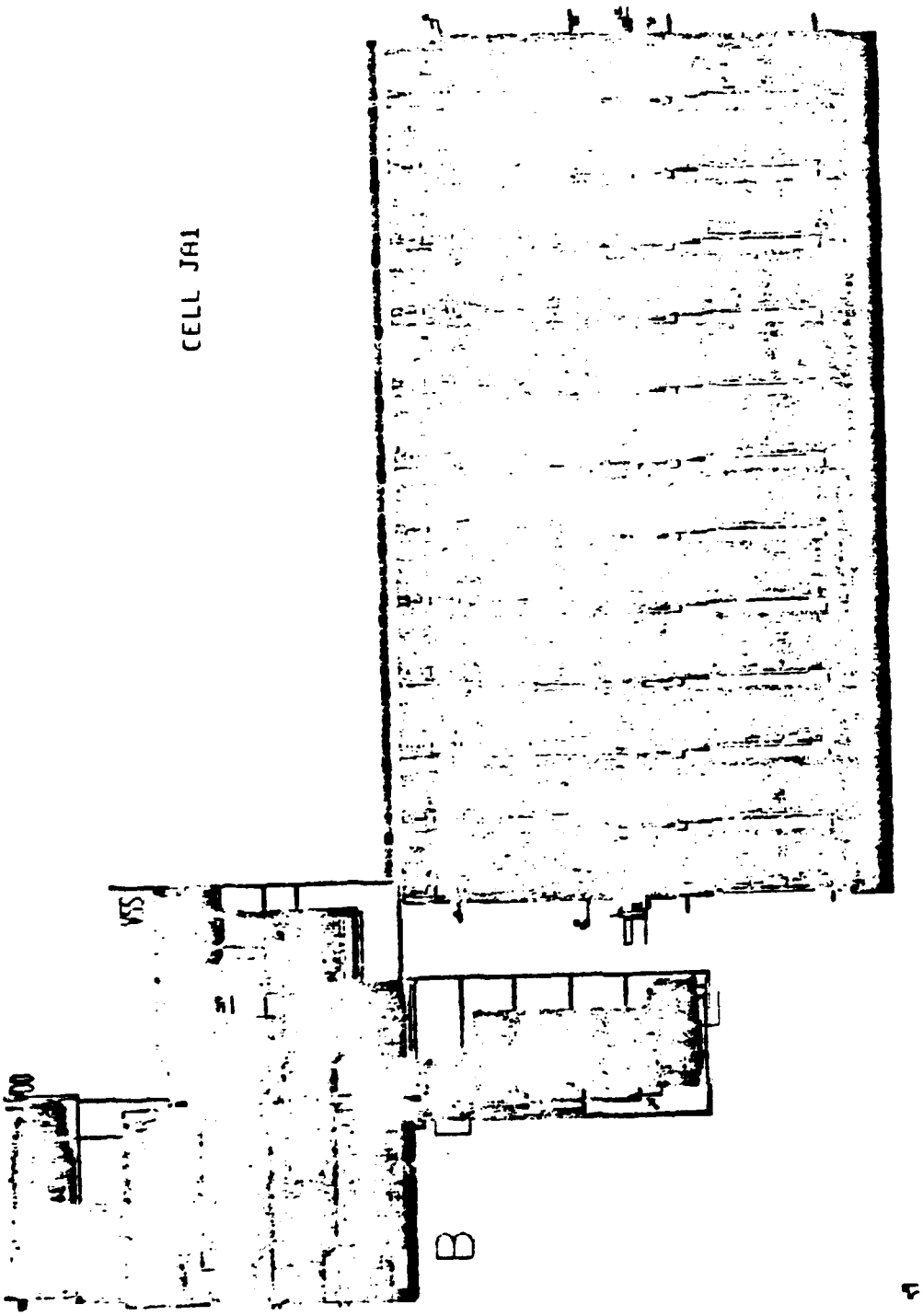

CELL JA7
JA8
1570X
1570X
1570X
1570X
1660X
1120X
1680X
VDD

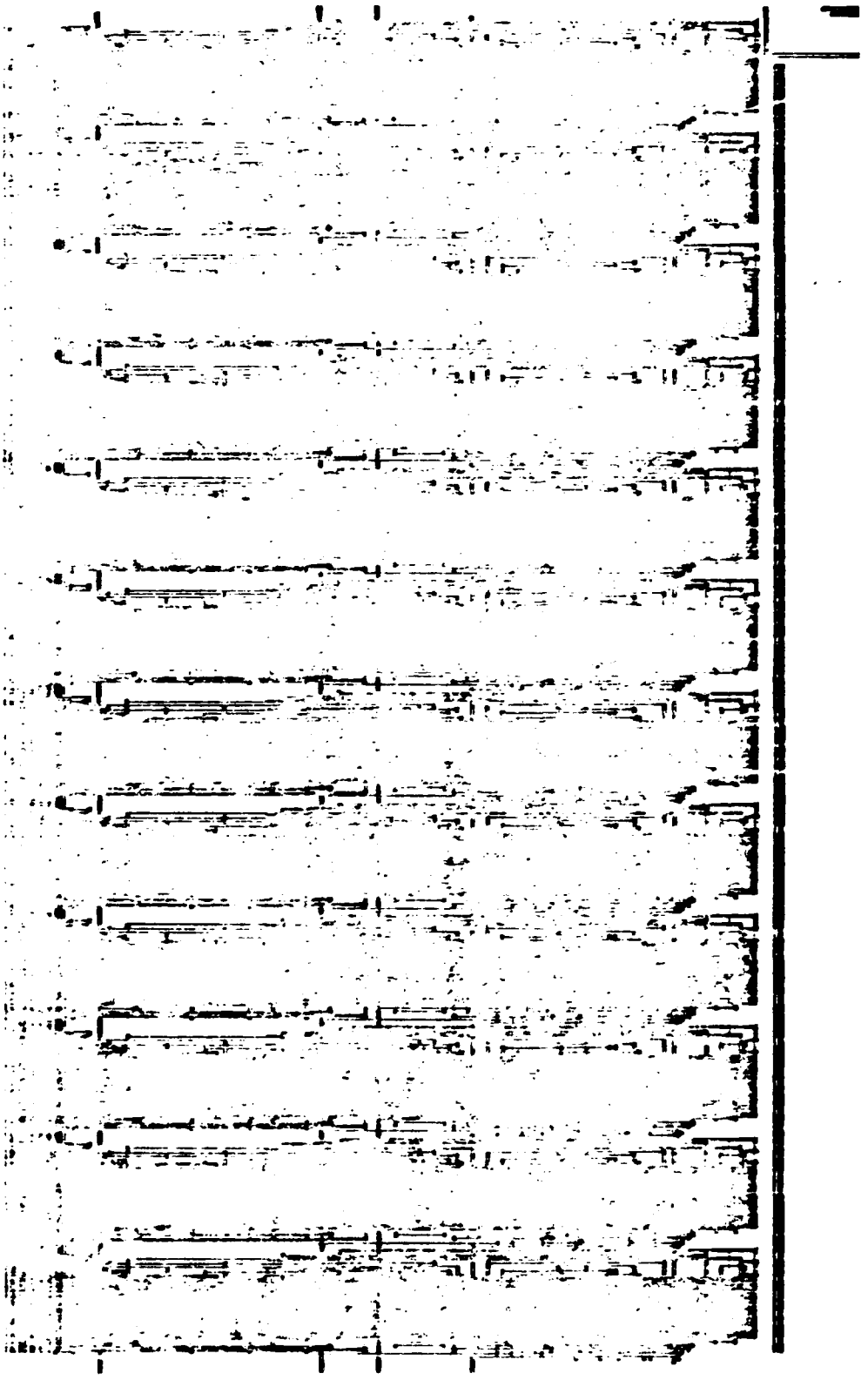

1766X
CELL JA8
JA9
ALL - 1220X
RN
RN

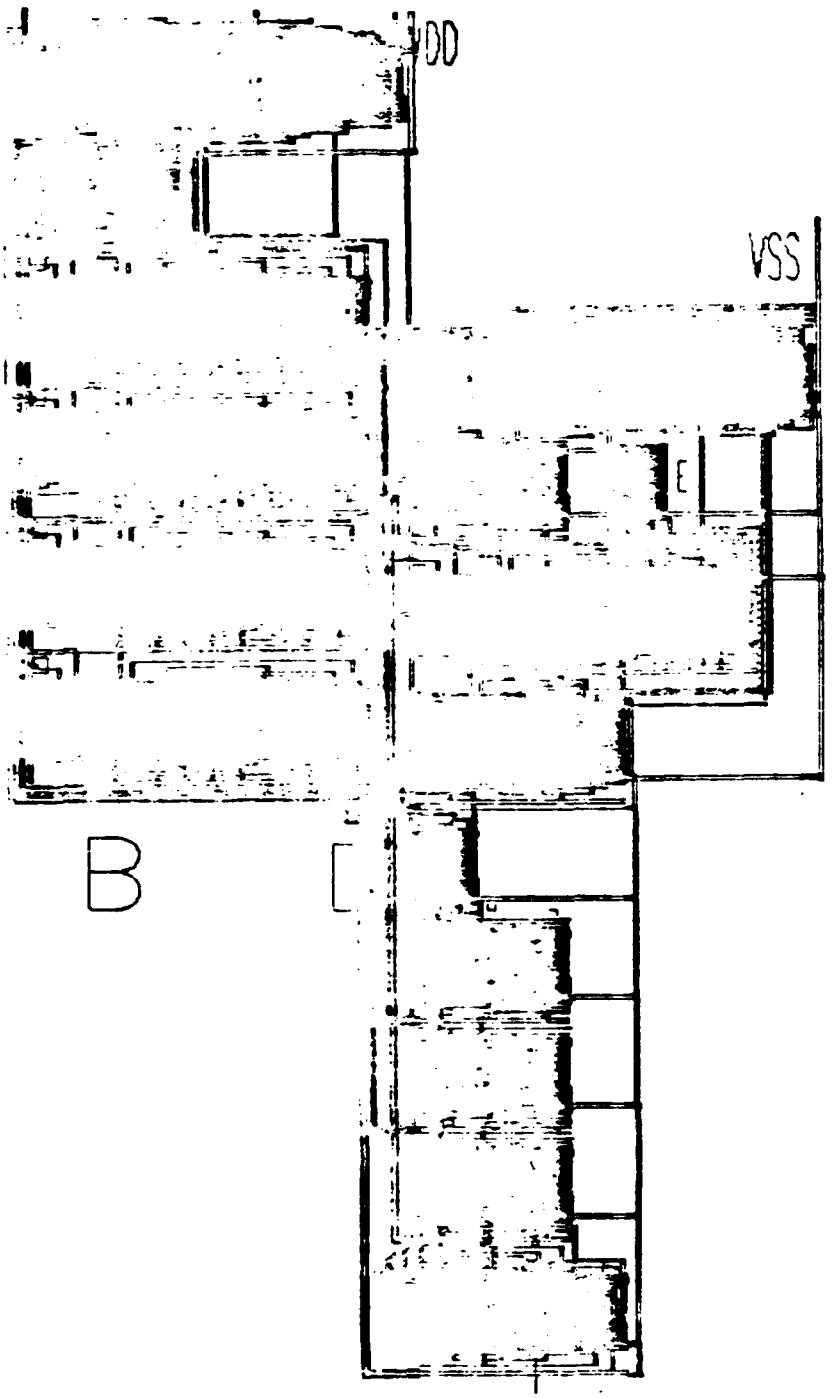

JA9
1660X
1120X
1740X
1140X
1130X
1130X
1670X
1670X
1760X
1660X
1760X
1660X
1120


JAIN
U
P
1120X
1220X
1760X
1220X
1760X

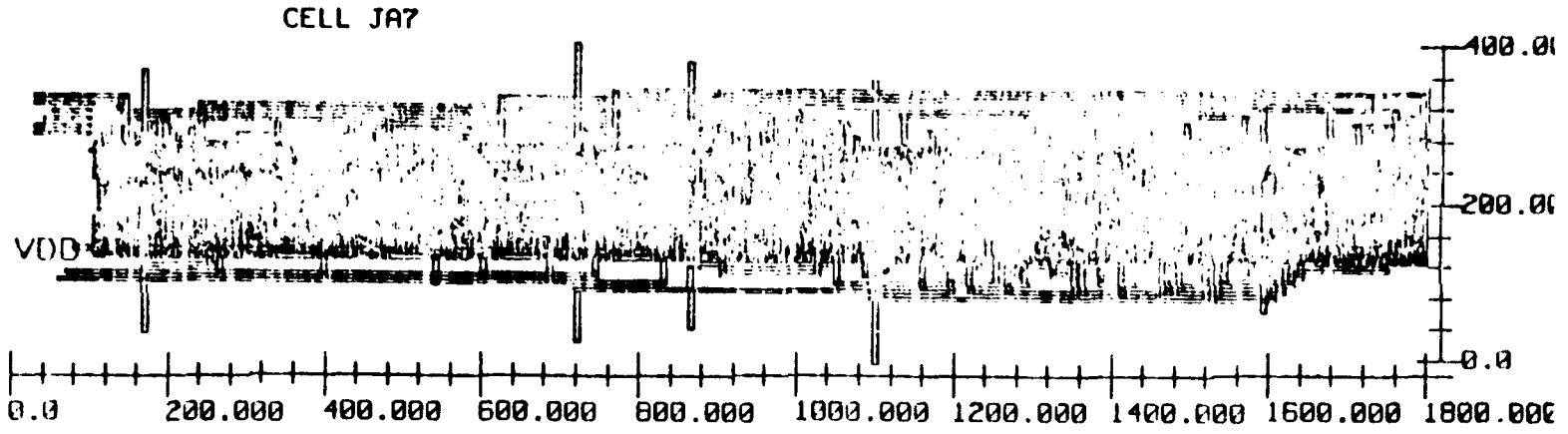

P
U
JA12
1220X
1680X
1760X
1760X
1760X
1760X
1220X
1120X


CELL JAIL
B





CELL JA6


CELL JA7
VDD
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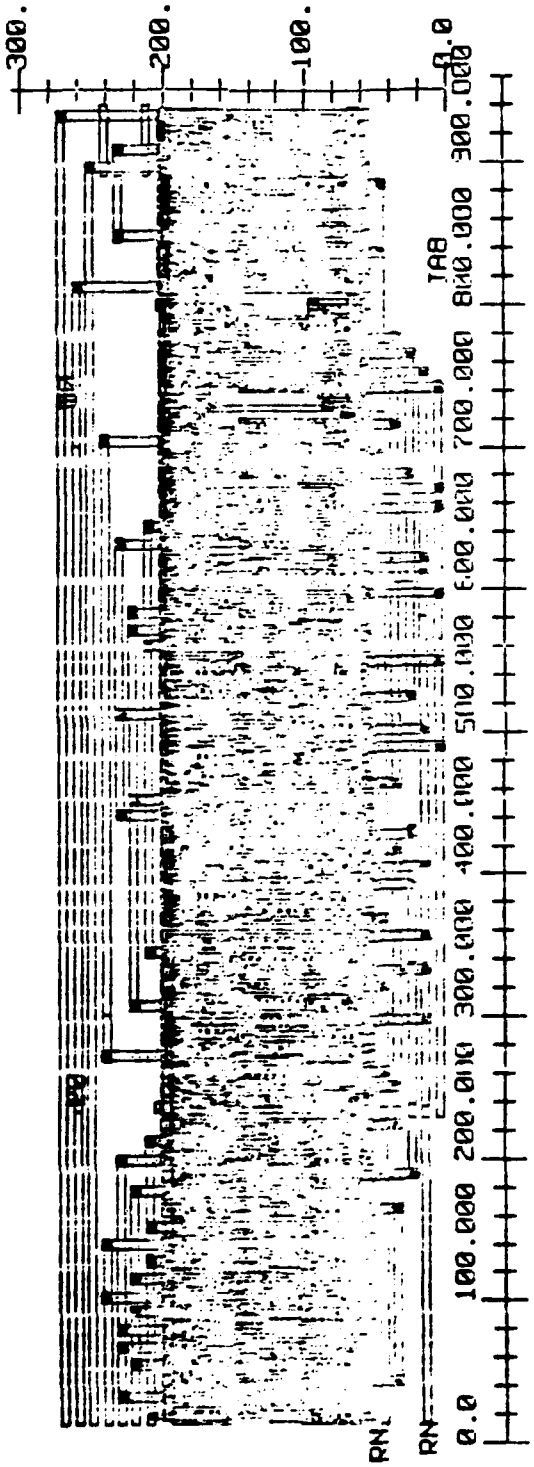
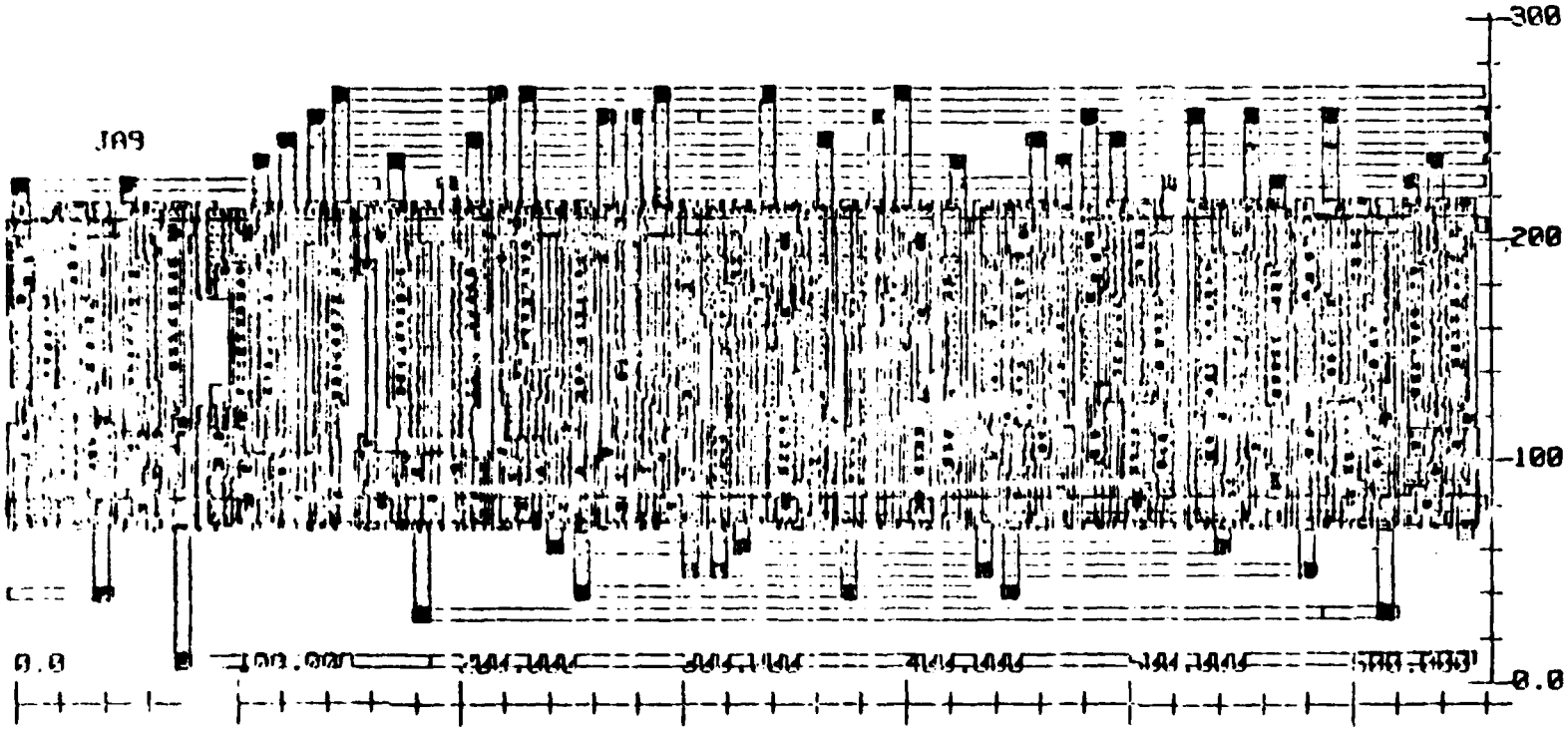
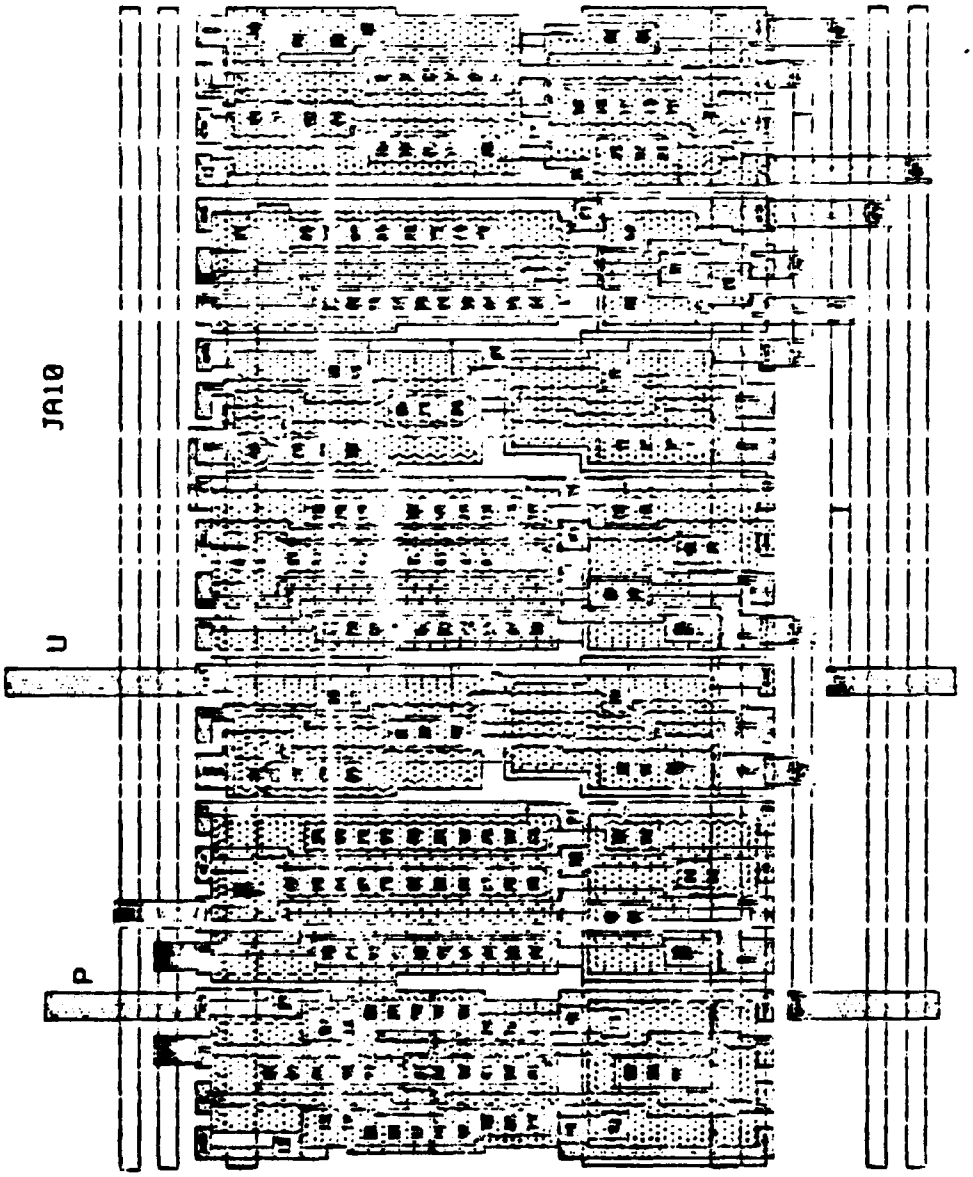
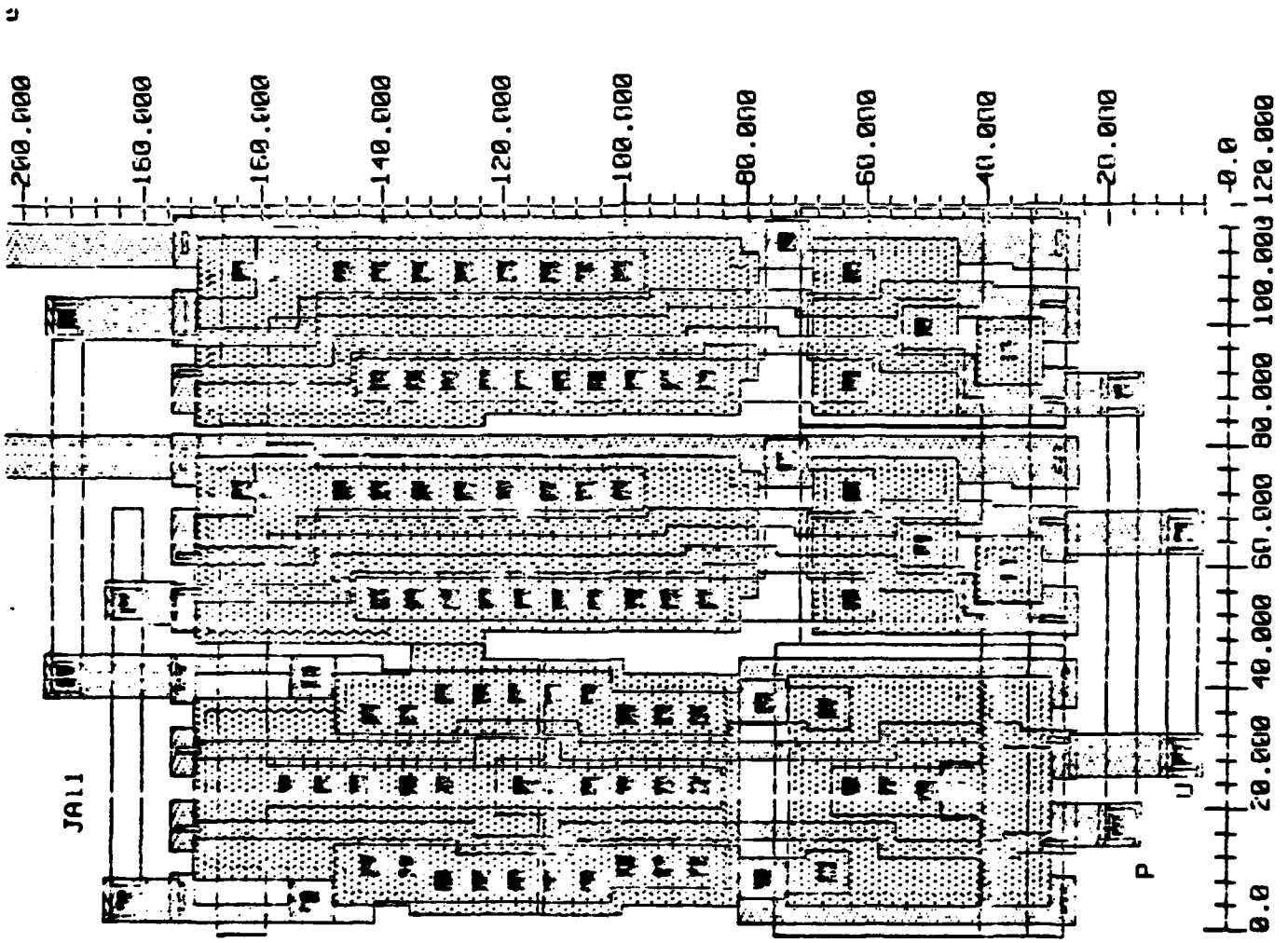
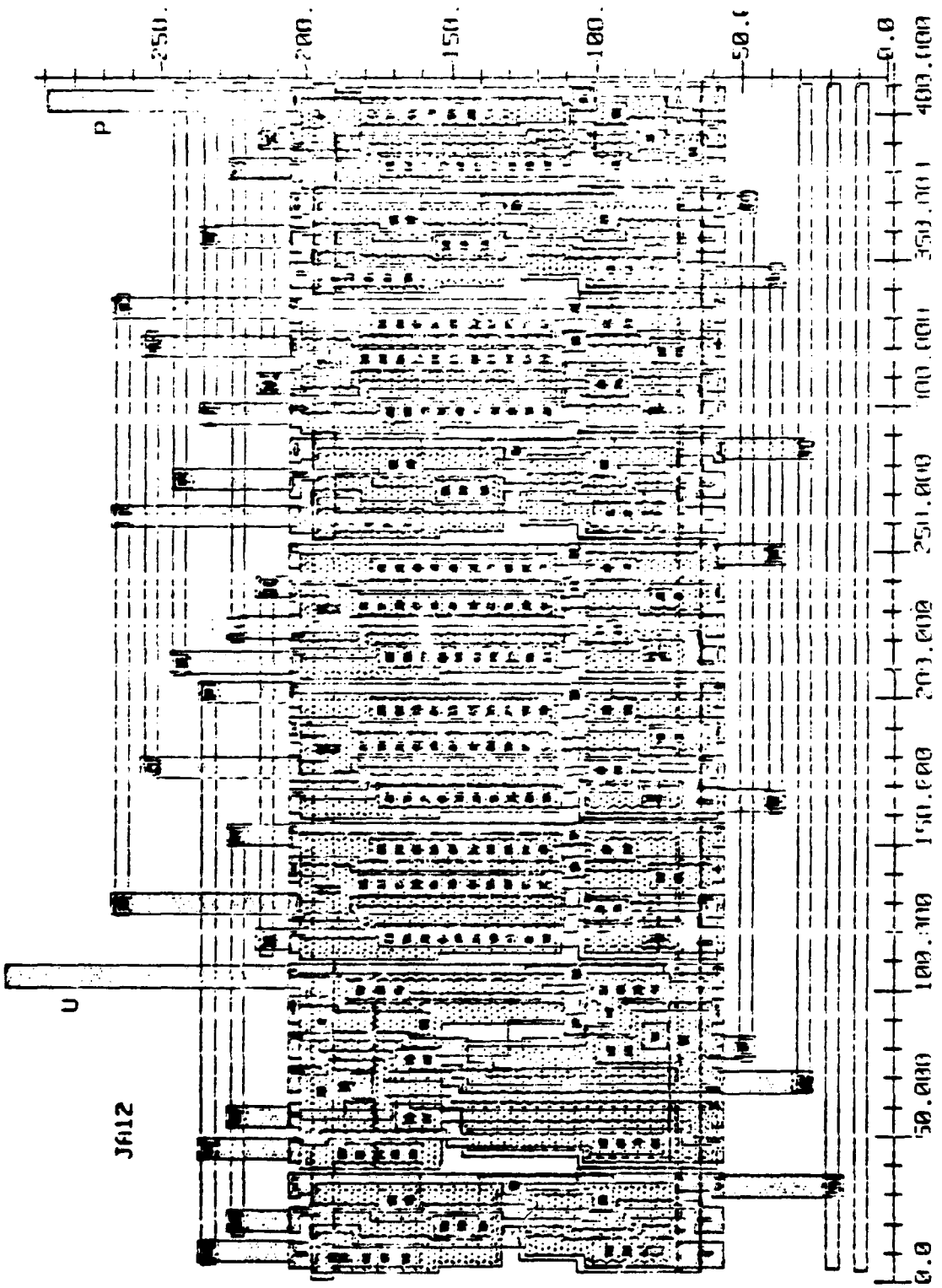
200.0
0.0
0.0
200.000
400.000
600.000
800.000
1000.000
1200.000
1400.000
1600.000
1800.000


300.
200.
100.
0.0
TAB
0.0
100.000
200.000
300.000
400.000
500.000
600.000
700.000
800.000
900.000
RN
RN


300
200
100
0.0
0.0


JA10
U
P


200.000
160.000
140.000
120.000
100.000
80.000
60.000
40.000
20.000
0.0
0.0
20.000
40.000
60.000
80.000
100.000
120.000
JA11


P
U
J612
250.
200.
150.
100.
50.0
0.0
400.000
350.000
300.000
250.000
200.000
150.000
100.000
50.0000
0.0

```
M326 38 31 32 33 CMOSP L=3U W=38U
M327 32 35 38 32 CMOSP L=3U W=30U
M3[illegible] 32 37 [illegible] 0 CMOSN L=3U W=42U
M357 39 36 310 0 CMOSN L=3U W=42U
M355 310 31 0 0 CMOSN L=3U W=6U
.ENDS INV3
.SUBCKT INV4 41 42 43
M428 42 41 43 43 CMOSP L=3U W=75.5U
M453 42 41 0 0 CMOSN L=3U W=6U
.ENDS INV4
.SUBCKT INV5 51 52 53
*NODES: IN. OUT. VDD
M534 52 51 53 53 CMOSP L=3U W=32U
M554 51 52 0 0 CMOSN L=3U W=6U
.ENDS INV5
.SUBCKT REF6 61 62 63 65 66 67
*NODES: IN. OUT. VDD. CS. CBAR6. R7
M629 62 67 63 63 CMOSP L=3U W=44U
M629 68 61 63 63 CMOSP L=3U W=7U
M631 62 66 68 63 CMOSP L=3U W=7U
M641 62 65 69 0 CMOSN L=3U W=6U
M660 67 67 610 0 CMOSN L=3U W=6U
M659 610 61 0 0 CMOSN L=3U W=6U
.ENDS REF6
.SUBCKT REF7 71 72 73 75 76 77
*NODES: IN. OUT. VDD. CS. CBAR6. R7
M723 78 77 73 73 CMOSP L=3U W=20U
M724 79 71 73 73 CMOSP L=3U W=9U
M725 711 75 78 73 CMOSP L=3U W=9U
M735 79 75 79 73 CMOSP L=3U W=20U
M755 7[illegible] 76 [illegible] 0 CMOSN L=3U W=6U
M714 710 71 711 0 CMOSN L=3U W=6U
M751 711 77 73 73 CMOSN L=3U W=6U
.ENDS REF7
.SUBCKT CLOCK8 81 83 85 86
*NODES: IN. VDD. CS. CBAR6
M832 8[illegible] 8[illegible] 83 83 CMOSP L=3U W=44.5U
M833 85 86 83 83 CMOSP L=3U W=44.5U
M862 86 81 0 0 CMOSN L=3U W=30U
M858 85 86 0 0 CMOSN L=3U W=25.5U
.ENDS CLOCK8
*1580 FIRST STAGE
X1 1 2 100 5 6 INV1
X2 2 3 100 0 INV2
X7 3 2 100 5 6 7 REF7
X3 3 4 100 5 6 7 INV3
X4 4 8 100 INV4
X5 8 9 100 INV5
X6 8 4 100 5 6 7 REF6
X9 10 100 5 6 CLOCK8
VI 100 0 PWL(0 0 3NS 5)
VIN 1 0 PWL(0 5 18NS 5 22NS 0 48NS 0 5[illegible]NS 5)
VC 10 0 PWL(0 0 10[illegible] 0 15NS 5 25NS 5 30NS 0 40NS 0 45NS 5 55NS 5 60NS 0)
* VC 10 0 PWL(0 0 5NS 0 9NS 5 11NS 5 15NS 0)
VR 7 0 DC 4.5
* .NODESET V(2)=5 V(3)=0 V(4)=5 V(8)=0 V(9)=5
.TRAN 1NS 70NS 0
.PRINT TRAN V(1) V(10) V(3) V(2) V(4) V(8) (-1.12)
* PLOT VOLTAGE RANGE GIVES NICE PRINTOUT
* [illegible]1.2 SOME EXPTS. USING PWL VDD
.P[illegible] TRAN V(1) V(10) V(3) V(2) V(4) V(8)
.P[illegible] 10[illegible]
.E[illegible]
```

UNFOLD

FIGURE 7

```
.MODEL CMOSN NMOS LEVEL=2.00000 LD=0.280000U TOX=500.00E-10 NSUB=1.000000E+16
+ VTO=0.827125 KP=3.286649E-05 GAMMA=1.35960  PHI=0.600000 UO=700.000
+ UCRIT=999000  DELTA=1.24050 VMAX=100000 XJ=0.400000U LAMBDA=1.604983E-2
+ NFS=1.234795E+12 NEFF=1.001000E-02 NSS=0.000000E+00 TPG=1.00000 RSH=25
+ CGSO=5.2E-10 CGDO=5.2E-10 CJ=3.2E-4 MJ=0.5 CJSW=9E-10 MJSW=0.33 UEXP=1.001E-
.MODEL CMOSP PMOS LEVEL=2.00000 LD=0.280000U TOX=500.000E-10 NSUB=1.121082E+14
+ VTO=-0.894654 KP=1.526452E-05 GAMMA=0.879003 PHI=0.600000 UO=100.000
+ UCRIT=16376.5 DELTA=1.93831 VMAX=100000 XJ=0.400000U LAMBDA=4.708659E-02
+ NFS=8.7E+617E+11 NEFF=1.001000E-02 NSS=0.000000E+00 TPG=-1.00000 RSH=55
+ CGSO=4E-10 CGDO=4E-10 CJ=2E-4 MJ=0.5 CJSW=4.5E-10 MJSW=0.33 UEXP=0.15441
.SUBCKT INV1 11 12 13 15 16
*NODES: INPUT.OUTPUT.VDD.C.CBAR
M111 17 11 13 13 CMOSP L=3U W=67U
*TRANS NODES D.G.S.B
M112 12 16 17 13 CMOSP L=3U W=65U
M121 12 15 18 0 CMOSN L=3U W=38U
M122 18 11 0 0 CMOSN L=3U W=49U
.ENDS INV1
.SUBCKT INV2 21 22 23
*NODES: INPUT.OUTPUT.VDD
M211 22 21 23 23 CMOSP L=3U W=48U
M212 22 21 0 0 CMOSN L=3U W=30U
.ENDS INV2
.SUBCKT INV3 31 32 33 35 36 37
*NODES: IN. OUT. VDD. CS. CBAR6. R7
M31 - 36 31 33 33 CMOSP L=3U W=35U
M313 32 31 35 32 CMOSP L=3U W=30U
M3 - 35 - 3. 0 CMOSN L=3U W=42U
M312 32 31 0 0 CMOSN L=3U W=42U
M313 35 31 0 0 CMOSN L=3U W=60U
.ENDS INV3
.SUBCKT INV4 41 42 43
M411 42 41 43 43 CMOSP L=3U W=75.5U
M412 42 41 0 0 CMOSN L=3U W=60U
.ENDS INV4
.SUBCKT INV5 51 52 53
*NODES: IN. OUT. VDD
M511 51 51 53 53 CMOSP L=3U W=33U
M512 51 51 0 0 CMOSN L=3U W=60U
.ENDS INV5
.SUBCKT BUFA 61 62 63 65 66 67
*NODES: IN. OUT. VDD. CS. CBAR6. R7
M611 66 67 63 63 CMOSP L=3U W=44U
M612 65 66 63 63 CMOSP L=3U W=7U
M613 62 66 63 63 CMOSP L=3U W=7U
M614 62 65 65 0 CMOSN L=3U W=6U
M615 66 67 61 0 CMOSN L=3U W=6U
M616 61 61 0 0 CMOSN L=3U W=6U
.ENDS BUFA
.SUBCKT BUFB 71 72 73 75 76 77
*NODES: IN. OUT. VDD. CS. CBAR6. R7
M711 76 77 73 73 CMOSP L=3U W=20U
M712 75 71 73 73 CMOSP L=3U W=9U
M713 72 75 73 73 CMOSP L=3U W=9U
M714 72 75 73 73 CMOSP L=3U W=20U
M715 72 76 0 0 CMOSN L=3U W=6U
M716 76 71 0 0 CMOSN L=3U W=6U
M717 75 77 0 0 CMOSN L=3U W=6U
.ENDS BUFB
```


UNFOLD

URE 7

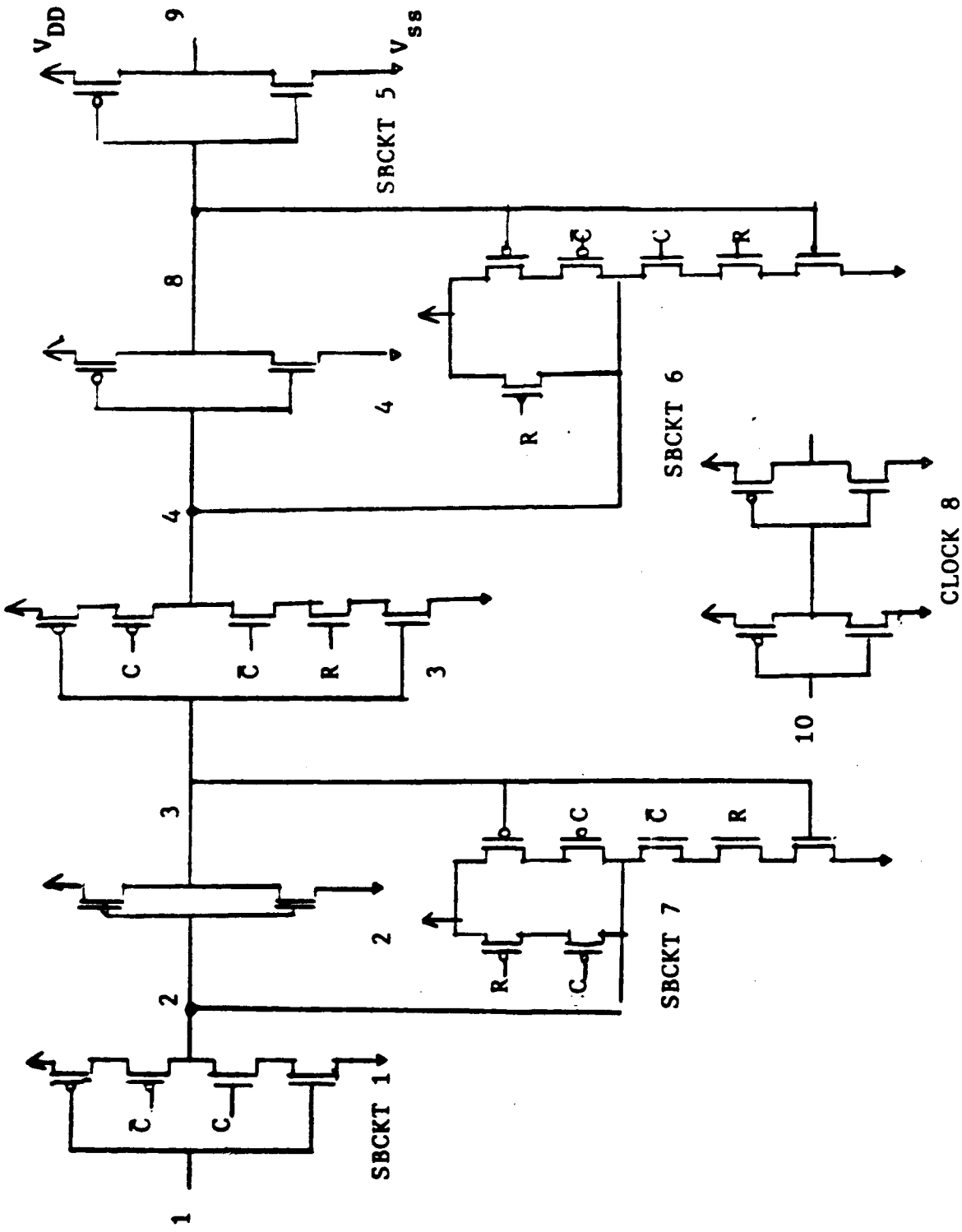


FIGURE 8 D Flip-flop Circuit

LEGEND:

*: V(1)
+: V(3)
=: V(2)

TIME	V(1)
(*+=)----------	-1.000E+00
0.	0.
2.000E-10	1.000E+00
4.000E-10	2.000E+00
6.000E-10	3.000E+00
8.000E-10	4.000E+00
1.000E-09	5.000E+00
1.200E-09	5.000E+00
1.400E-09	5.000E+00
1.600E-09	5.000E+00
1.800E-09	5.000E+00
2.000E-09	5.000E+00
2.200E-09	5.000E+00
2.400E-09	4.000E+00
2.600E-09	3.000E+00
2.800E-09	2.000E+00
3.000E-09	1.000E+00
3.200E-09	-1.297E-13
3.400E-09	0.
3.600E-09	0.
3.800E-09	0.
4.000E-09	0.
4.200E-09	0.
4.400E-09	1.000E+00
4.600E-09	2.000E+00
4.800E-09	3.000E+00
5.000E-09	4.000E+00
5.200E-09	5.000E+00
5.400E-09	5.000E+00
5.600E-09	5.000E+00
5.800E-09	5.000E+00
6.000E-09	5.000E+00
6.200E-09	5.000E+00
6.400E-09	3.333E+00
6.600E-09	1.667E+00
6.800E-09	0.
7.000E-09	0.
7.200E-09	0.
7.400E-09	0.
7.600E-09	1.667E+00
7.800E-09	3.333E+00
8.000E-09	5.000E+00
8.200E-09	5.000E+00
8.400E-09	5.000E+00
8.600E-09	5.000E+00
8.800E-09	5.000E+00
9.000E-09	5.000E+00
9.200E-09	5.000E+00
9.400E-09	5.000E+00
9.600E-09	5.000E+00
9.800E-09	5.000E+00
1.000E-08	5.000E+00

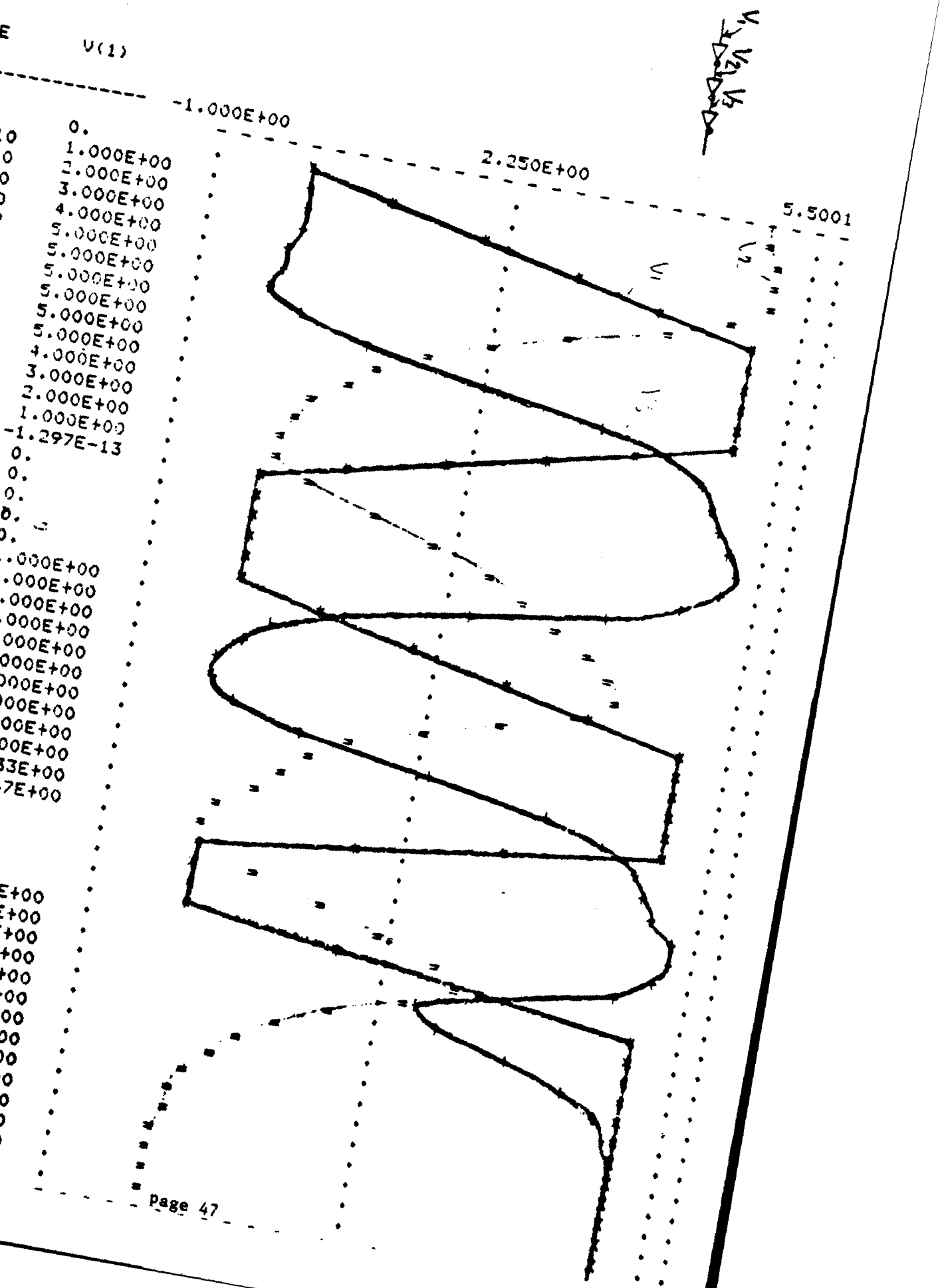


FIGURE 6

LEGEND:

*: V(1)
+: V(3)
=: V(2)

TIME	V(1)
0.	0.
2.000E-10	1.000E+00
4.000E-10	2.000E+00
6.000E-10	3.000E+00
8.000E-10	4.000E+00
1.000E-09	5.000E+00
1.200E-09	5.000E+00
1.400E-09	5.000E+00
1.600E-09	5.000E+00
1.800E-09	5.000E+00
2.000E-09	5.000E+00
2.200E-09	4.000E+00
2.400E-09	3.000E+00
2.600E-09	2.000E+00
2.800E-09	1.000E+00
3.000E-09	-1.279E-13
3.200E-09	0.
3.400E-09	0.
3.600E-09	0.
3.800E-09	0.
4.000E-09	0.
4.200E-09	1.000E+00
4.400E-09	2.000E+00
4.600E-09	3.000E+00
4.800E-09	4.000E+00
5.000E-09	5.000E+00
5.200E-09	5.000E+00
5.400E-09	5.000E+00
5.600E-09	5.000E+00
5.800E-09	5.000E+00
6.000E-09	5.000E+00
6.200E-09	3.333E+00
6.400E-09	1.667E+00
6.600E-09	0.
6.800E-09	0.
7.000E-09	0.
7.200E-09	0.
7.400E-09	1.667E+00
7.600E-09	3.333E+00
7.800E-09	5.000E+00
8.000E-09	5.000E+00
8.200E-09	5.000E+00
8.400E-09	5.000E+00
8.600E-09	5.000E+00
8.800E-09	5.000E+00
9.000E-09	5.000E+00
9.200E-09	5.000E+00
9.400E-09	5.000E+00
9.600E-09	5.000E+00
9.800E-09	5.000E+00
1.000E-08	5.000E+00

(*+=)---------- -1.000E+00 2.250E+00 5.500

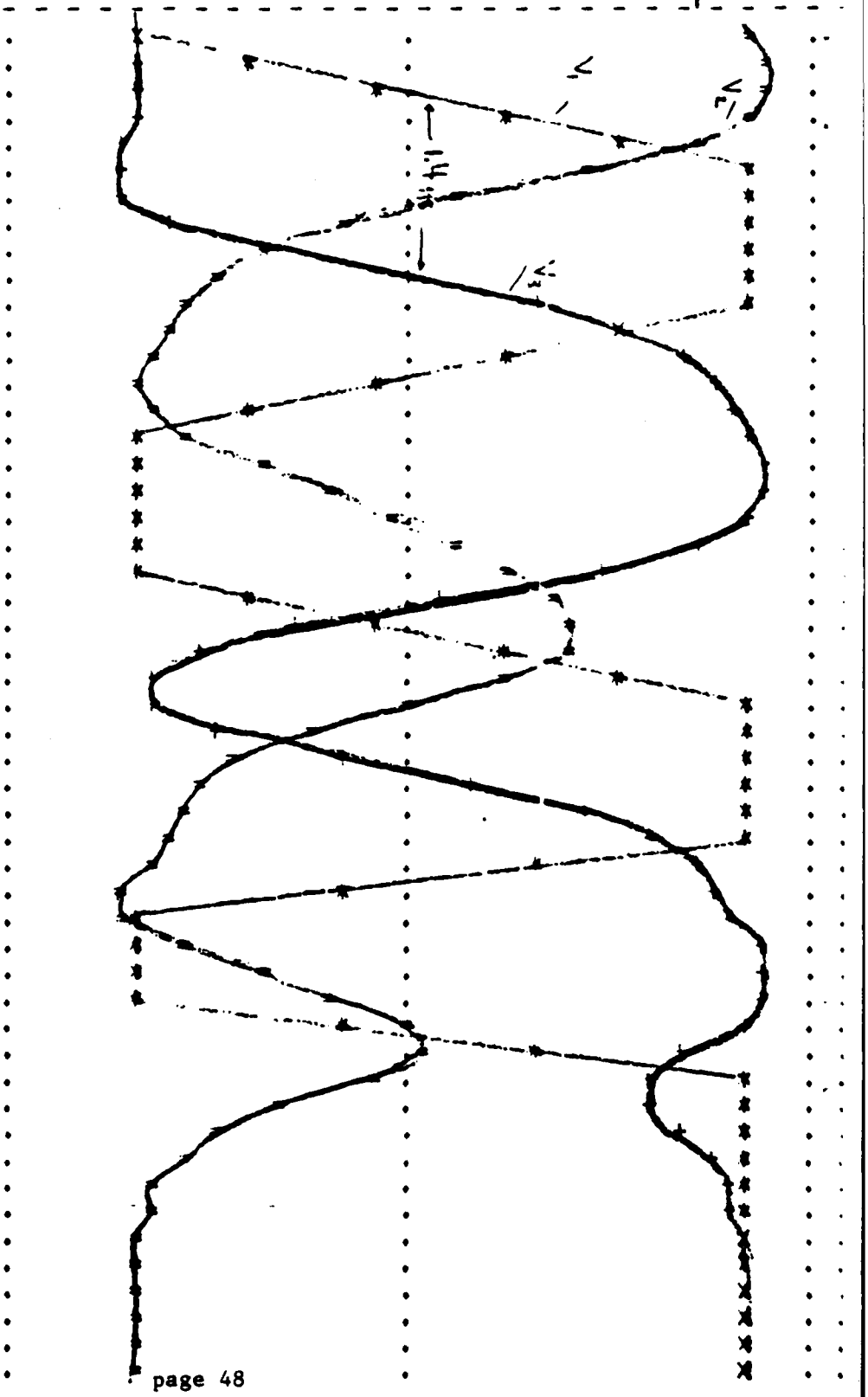
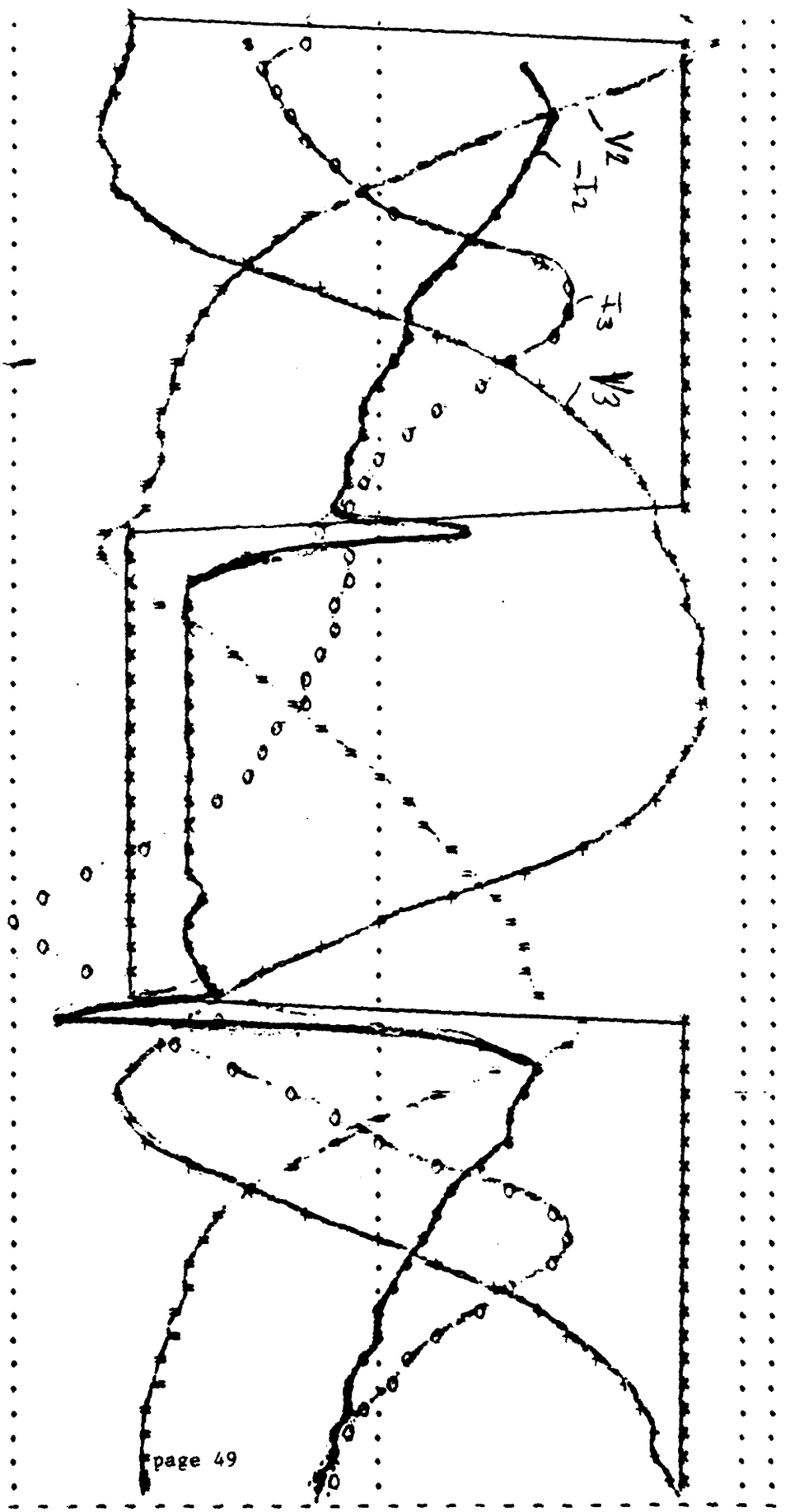


FIGURE 10

0.	0.
1.000E-10	5.000E+00
2.000E-10	5.000E+00
3.000E-10	5.000E+00
4.000E-10	5.000E+00
5.000E-10	5.000E+00
6.000E-10	5.000E+00
7.000E-10	5.000E+00
8.000E-10	5.000E+00
9.000E-10	5.000E+00
1.000E-09	5.000E+00
1.100E-09	5.000E+00
1.200E-09	5.000E+00
1.300E-09	5.000E+00
1.400E-09	5.000E+00
1.500E-09	5.000E+00
1.600E-09	5.000E+00
1.700E-09	5.000E+00
1.800E-09	5.000E+00
1.900E-09	5.000E+00
2.000E-09	5.000E+00
2.100E-09	0.
2.200E-09	0.
2.300E-09	0.
2.400E-09	0.
2.500E-09	0.
2.600E-09	0.
2.700E-09	0.
2.800E-09	0.
2.900E-09	0.
3.000E-09	0.
3.100E-09	0.
3.200E-09	0.
3.300E-09	0.
3.400E-09	0.
3.500E-09	0.
3.600E-09	0.
3.700E-09	0.
3.800E-09	0.
3.900E-09	0.
4.000E-09	0.
4.100E-09	5.000E+00
4.200E-09	5.000E+00
4.300E-09	5.000E+00
4.400E-09	5.000E+00
4.500E-09	5.000E+00
4.600E-09	5.000E+00
4.700E-09	5.000E+00
4.800E-09	5.000E+00
4.900E-09	5.000E+00
5.000E-09	5.000E+00
5.100E-09	5.000E+00
5.200E-09	5.000E+00
5.300E-09	5.000E+00
5.400E-09	5.000E+00
5.500E-09	5.000E+00
5.600E-09	5.000E+00
5.700E-09	5.000E+00
5.800E-09	5.000E+00
5.900E-09	5.000E+00
6.000E-09	5.000E+00

FIGURE 11

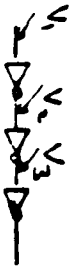
UNFOLD



OLEGEND:

*: V(1)
+: V(3)
=: V(2)
$: I(V02)
O: I(V03)

TIME	V(1)
(*+=)----------	-1.000E+00 2.250E+00 5.500
($O)----------	-2.000E-04 5.000E-05 3.000
0.	0.
1.000E-10	5.000E+00
2.000E-10	5.000E+00
3.000E-10	5.000E+00
4.000E-10	5.000E+00
5.000E-10	5.000E+00
6.000E-10	5.000E+00
7.000E-10	5.000E+00
8.000E-10	5.000E+00
9.000E-10	5.000E+00
1.000E-09	5.000E+00
1.100E-09	5.000E+00
1.200E-09	5.000E+00
1.300E-09	5.000E+00
1.400E-09	5.000E+00
1.500E-09	5.000E+00
1.600E-09	5.000E+00
1.700E-09	5.000E+00
1.800E-09	5.000E+00
1.900E-09	5.000E+00
2.000E-09	5.000E+00
2.100E-09	0.
2.200E-09	0.
2.300E-09	0.
2.400E-09	0.
2.500E-09	0.
2.600E-09	0.
2.700E-09	0.
2.800E-09	0.
2.900E-09	0.
3.000E-09	0.
3.100E-09	0.
3.200E-09	0.
3.300E-09	0.
3.400E-09	0.
3.500E-09	0.
3.600E-09	0.
3.700E-09	0.
3.800E-09	0.
3.900E-09	0.
4.000E-09	0.
4.100E-09	5.000E+00
4.200E-09	5.000E+00
4.300E-09	5.000E+00



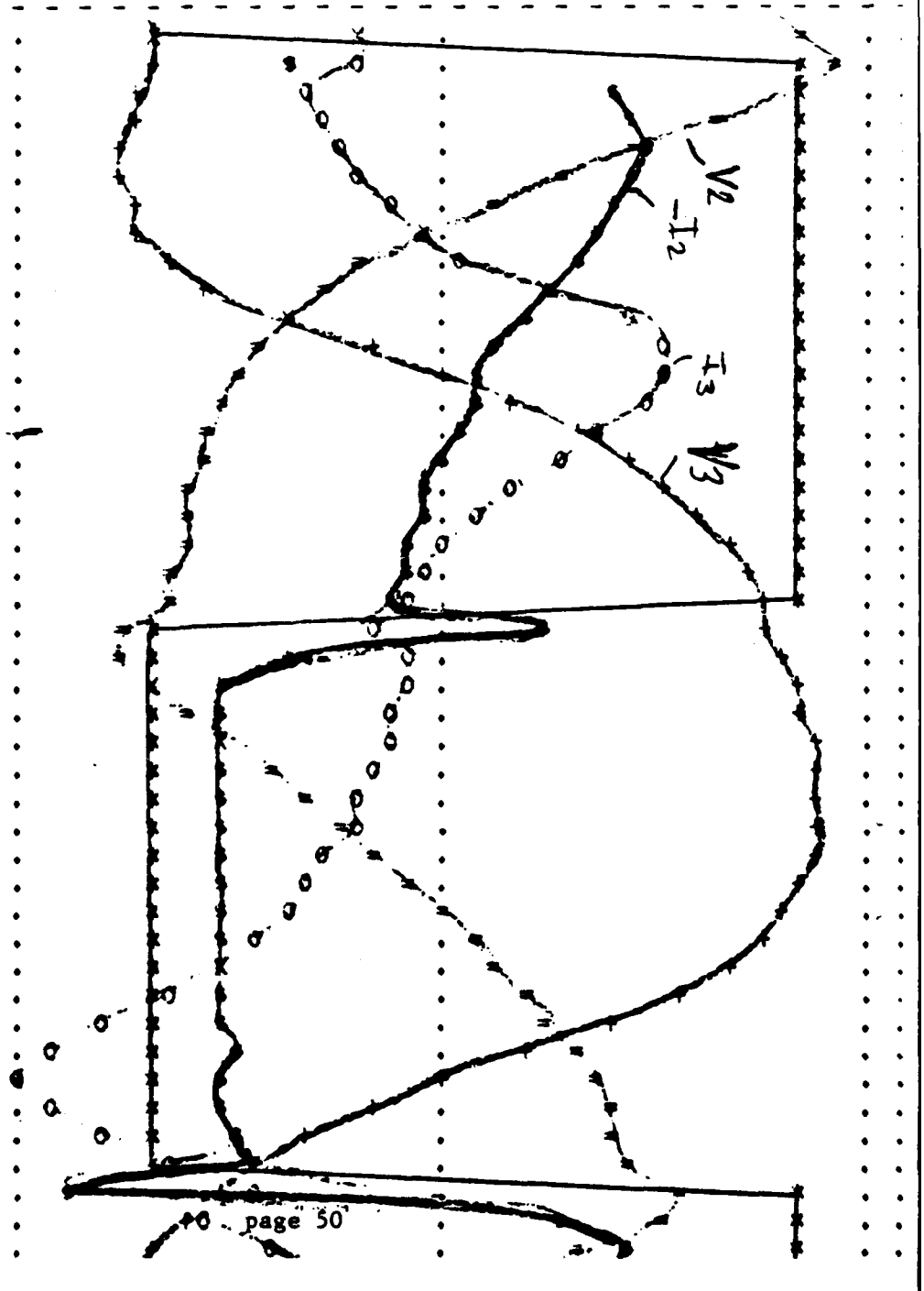
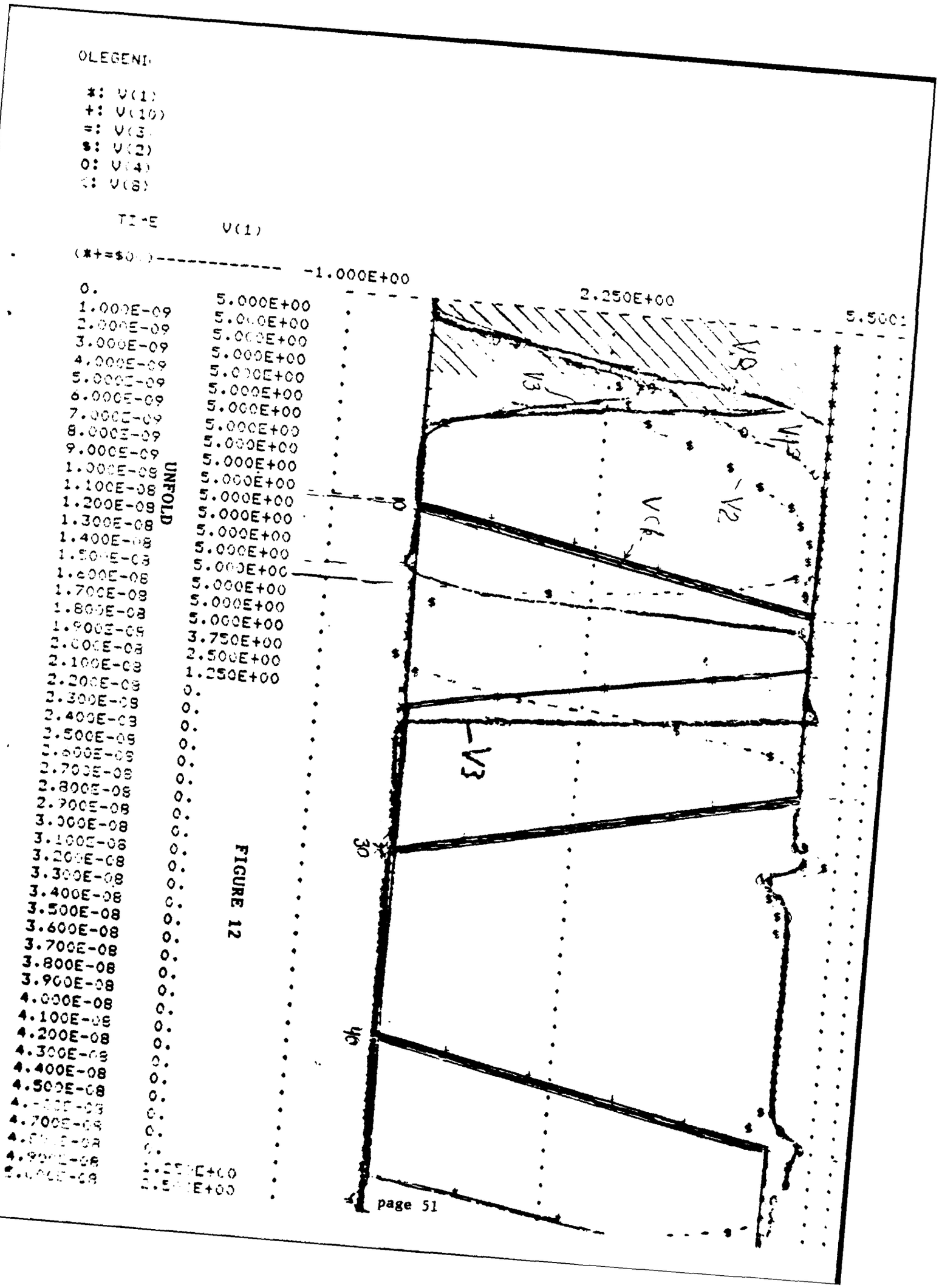


FIGURE 11

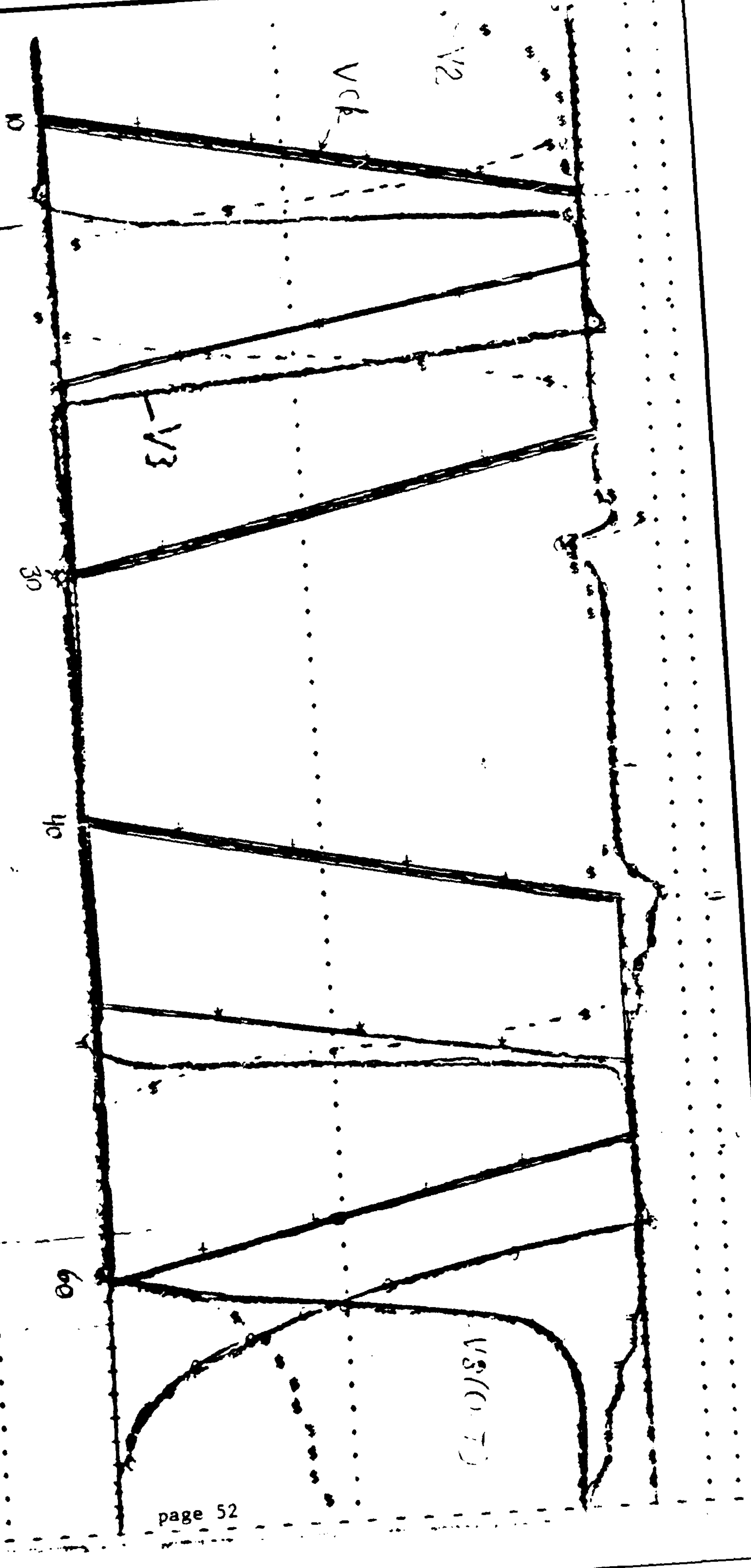
UNFOLD


LEGEND:
*: V(1)
+: V(10)
=: V(3)
$: V(2)
0: V(4)
<: V(6)
TIME
V(1)
-1.000E+00
2.250E+00
5.500E+00
UNFOLD
FIGURE 12

UNFOLD

[illegible]	[illegible]
8.000E-09	5.000E+00
9.000E-09	5.000E+00
1.000E-08	5.000E+00
1.100E-08	5.000E+00
1.200E-08	5.000E+00
1.300E-08	5.000E+00
1.400E-08	5.000E+00
1.500E-08	5.000E+00
1.600E-08	5.000E+00
1.700E-08	5.000E+00
1.800E-08	5.000E+00
1.900E-08	3.750E+00
2.000E-08	2.500E+00
2.100E-08	1.250E+00
2.200E-08	0.
2.300E-08	0.
2.400E-08	0.
2.500E-08	0.
2.600E-08	0.
2.700E-08	0.
2.800E-08	0.
2.900E-08	0.
3.000E-08	0.
3.100E-08	0.
3.200E-08	0.
3.300E-08	0.
3.400E-08	0.
3.500E-08	0.
3.600E-08	0.
3.700E-08	0.
3.800E-08	0.
3.900E-08	0.
4.000E-08	0.
4.100E-08	0.
4.200E-08	0.
4.300E-08	0.
4.400E-08	0.
4.500E-08	0.
4.600E-08	0.
4.700E-08	0.
4.800E-08	0.
4.900E-08	1.250E+00
5.000E-08	2.500E+00
5.100E-08	3.750E+00
5.200E-08	5.000E+00
5.300E-08	5.000E+00
5.400E-08	5.000E+00
5.500E-08	5.000E+00
5.600E-08	5.000E+00
5.700E-08	5.000E+00
5.800E-08	5.000E+00
5.900E-08	5.000E+00
6.000E-08	5.000E+00
6.100E-08	5.000E+00
6.200E-08	5.000E+00
6.300E-08	5.000E+00
6.400E-08	5.000E+00
6.500E-08	5.000E+00
6.600E-08	5.000E+00
6.700E-08	5.000E+00
6.800E-08	5.000E+00
6.900E-08	5.000E+00
7.000E-08	5.000E+00

FIGURE 12



END
DATE
FILMED

12-8-87